A McGRAW-HILL PUBLICATION

THREE DOLLARS

Electronics

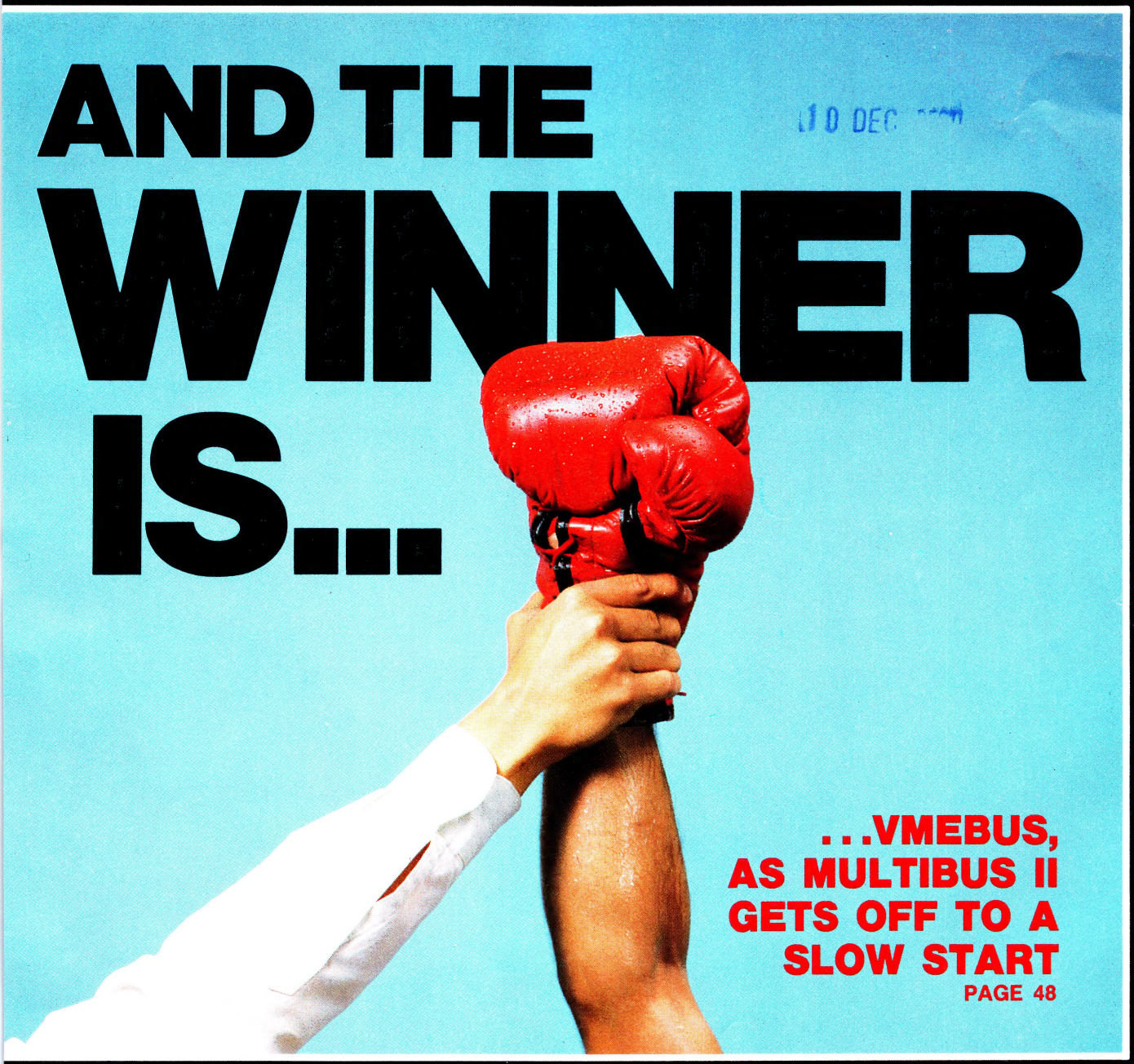
THE WORLDWIDE TECHNOLOGY WEEKLY

NOVEMBER 25, 1985

BATTLE OF THE BUSES

AND THE WINNER IS...

10 DEC



...VMEBUS, AS MULTIBUS II GETS OFF TO A SLOW START

PAGE 48

EXPERT SYSTEMS TACKLE VLSI TESTING/56

JAPAN AND KOREA: OLD ENEMIES UNITE TO COMPETE/62

SERIES 32000 IS A TRADEMARK OF NATIONAL SEMICONDUCTOR CORPORATION.
UNIX IS A TRADEMARK OF AT&T BELL LABORATORIES.

"We did it!"
"I knew we'd close that sale. Did you see their faces?"
"It's our competitors' faces I want to see. We've really cracked this market now."
"Looks like we made all the right decisions at the right times."
"Like National's 32-bit microprocessor family?"
"You can't build a system out of data sheets and promises. National had it, they delivered it, and they got us here first."
SERIES 32000
THE SUPERMINI ON A CHIP

While you're still dreaming about success, Sequent is delivering it. With National's Series 32000 family.

On January 17, 1983, eighteen people started a new company called Sequent Computer Systems. They had no product, no plan, no backing. Only a dream.

Two years later, that dream came true. They delivered their first system—a sophisticated parallel processing computer. A full year ahead of their competitors.

How'd they do it? Hard work. Calculated risks. Belief. And a critical decision. They chose the Series 32000™ microprocessor family.

It offered them a *complete* 32-bit microprocessor family, including demand paged virtual Memory Management, Floating Point, and other peripherals with full UNIX™ support.

But the Series 32000 wasn't just the right engineering decision, it was the right *business* decision. It helped Sequent get their system to market fast. First.

Sequent hit their window of opportunity. And that window is still open—for now. So find out how the Series 32000 can help you build your own success story. Contact National Semiconductor today.

National's Series 32000, MS 23-200
P.O. Box 58090
Santa Clara, CA 95052-8090

National Semiconductor
We're doing it.

Circle 1 on reader service card

In A Head-To-Head Power Meter Matchup, Boonton Wins!

BOONTON

Boonton's Model 4200 RF Microwattmeter has won over some very important customers in recent head-to-head comparisons with our major competitor. Consider the following —

Dual Channel Matchup: The Boonton 4200 is just that...two completely independent channels that provide simultaneous and continuous real-time differences of power levels...not two multiplexed front ends, like our competition, which can destroy the validity of swept measurements.

Basic Accuracy Matchup: The Boonton 4200 is calibrated to DC standards so the basic accuracy is 0.01 dB...that's twice as good as our competition. The 4200 also meets the environmental requirements of MIL-T-28800 C.

Frequency Coverage Matchup: The Boonton 4200 starts as low as 100 kHz and goes all the way to 75 GHz...soon to be 110 GHz. Coaxial type N inputs to 18 GHz, waveguide inputs for K, Ka, Q and V Bands and APC-3.5 adapters for K and Ka.

Sensitivity/Dynamic Range Matchup: The Boonton 4200 coaxial sensors cover −60 dBm to +30 dBm from 100 kHz to 18 GHz...individual sensors have up to 70 dB dynamic range. Even in the millimeter wave bands it has −50 dBm sensitivity and 60 dB dynamic range.

Sensor Interchangeability Matchup: The Boonton 4200 can store complete sensor data for up to 8 sensors ...that data includes up to 20 cal factors for each sensor which are automatically applied with frequency entry.

System Interfacing Matchup: The Boonton 4200 can make up to 20 measurements per second over the optional GPIB. An optional internal TMA provides MATE compatibility.

Contact your local representative or call Boonton directly for more information or a convincing demonstration.

☐ RF SIGNAL GENERATORS ☐ RF MILLIVOLTMETERS
☐ MODULATION METERS ☐ IMPEDANCE METERS & BRIDGES
☐ RF POWER METERS ☐ AUDIO OSCILLATORS

Boonton Electronics Corporation
791 Route 10, Randolph, NJ 07869
Telephone (201) 584-1077

Circle 2 on reader service card

NOVEMBER 25, 1985 VOLUME 58, NO. 47

Electronics

NEWS

Newsletters

Technology, 13
- Toshiba's HEMT will follow Gould's to market
- 3M and Optimem team up on optical-disk drive
- General Electric brings smart-power technology to the ASIC market

Electronics, 15
- Japanese memory makers face hard times
- Now AT&T puts its weight behind the VMEbus standard
- Motorola to replace mask ROMs with EPROMs

Integrated circuits, 18
Behind Motorola's silence: ambitious product plans including big plans for BiMOS technology

Military, 19
SIA proposes a board to work on reforming procurement practices

Computers, 19
- Going for the 60-gigaflops supermachine
- Fujitsu tops IBM's Sierra in price/performance

Semiconductors, 22
IBM fires hot electrons through cooled GaAs

Expert systems, 24
Physicians' AI tools still need doctoring

Peripherals, 26
Kodak raises its stake in mass storage with three high-density floppy drives

Components, 26
Three firms move to cut the cost of touch panels

Graphics, 28
Tardy UK board makers draw a bead on OEMs

Microcontrollers, 30
Made-to-order controller ICs move in

INSIDE TECHNOLOGY

Eight CRT beams paint with film-like detail, 35
A high-definition raster display generated by a bundle of thin electron beams simplifies switching and control at high data rates. Intended for interactive imaging systems, it combines standard components with a unique electro-optic setup

Minisupercomputer divides to conquer, 43
A high-performance scientific minisupercomputer sports up to five specially designed computational processors that can churn out 16 megaflops. A separate processor runs the operating system

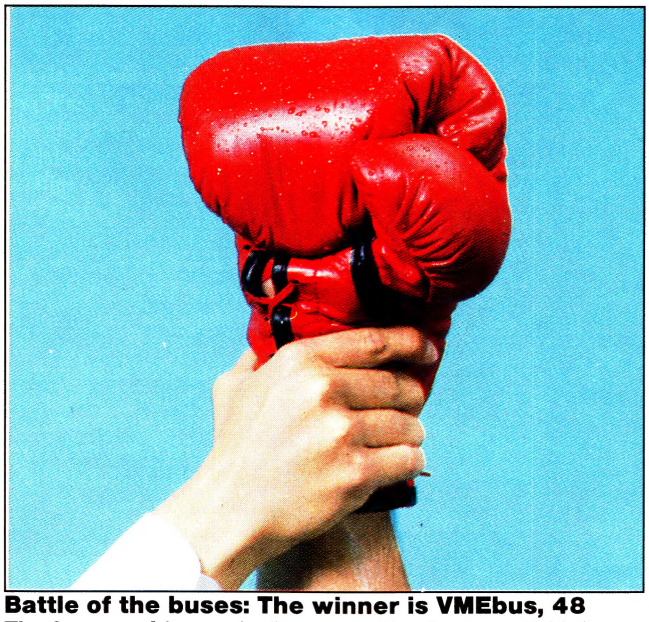
Expert systems tackle VLSI testing, 56
Designers of automatic test equipment are turning to expert systems as a way of helping users cope with the complexity of VLSI chips and boards

A pride of CPUs runs high-level languages, 58
Easier-to-use small computers based on artificial-intelligence techniques will likely result from the emergence of single-chip and board processors that run high-level languages directly

PROBING THE NEWS

Japan and Korea: old foes unite to compete, 62
Two countries that have been at each other's throats more often than not are forging a partnership in electronics. Many observers think the arrangement may be the wave of the future in electronics manufacturing

COVER



Battle of the buses: The winner is VMEbus, 48
The first round is over in the competition between 32-bit bus structures. VMEbus, with its three-year head start, is the clear winner over its nearest challenger, Multibus II
Cover design by Art Director Fred Sklenar

NEW PRODUCTS

Newsletter, 17
- PDP-11/83 is DEC's most powerful Q-bus computer
- Despite the odds, TI is stepping up its dynamic-RAM activities
- Superminicomputer from Integrated Digital Products executes 20 mips

Instruments, 71
Tektronix' portable analyzers boast a frequency range and level of intelligence typical of its more-expensive models

Integrated circuits, 71
Electroluminescent displays will get a boost from Siliconix's low-power drivers

DEPARTMENTS

Publisher's letter, 5

Meetings, 8

Companies, 64
Perkin-Elmer unleashes its Data Systems Group: now it's Concurrent Computer Corp.

Bottom lines, 65
Ameritech will buy software-giant Applied Data Research for $215 million

Electronics index, 67
The U. S. trade picture for electronic equipment continues to look bleak

People, 68
- Neil Vander Dussen is reorganizing Sony America to achieve flexibility
- Now Glenn Penisten manages seed-money funding
- People on the move

New literature, 77

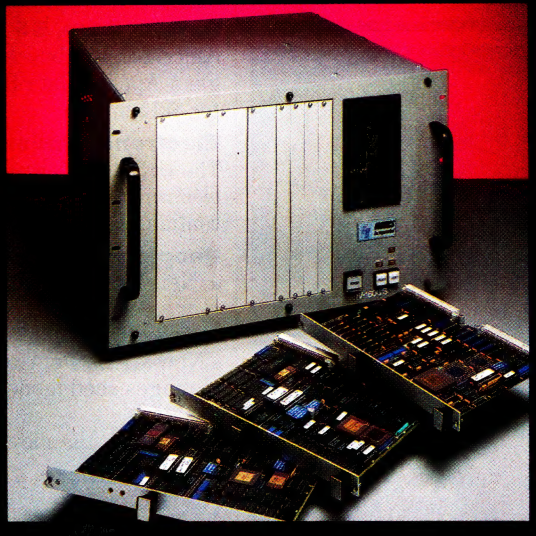
Letters, 79

Electronics week, 80
- A team of companies will develop a real-time operating system for Intel's 80386
- Sony beats Kodak to the punch with an optical disk

IRONICS HIGH PERFORMANCE VMEbus

THE ADVANCED MULTIPROCESSING ENVIRONMENT

Ironics, the high performance leader in VMEbus, announces the availability of the next generation of VMEbus CPU modules. Optimized for multiprocessing, these modules implement a standard set of hardware and software features that take full advantage of the VMEbus multimaster capabilities. For the first time, efficient interprocessor communication and syncronized data exchange make true high speed multiprocessing a reality. Features such as VMXbus interfaces, interrupters and interrupt handlers, fast dual-ported static and dynamic RAM arrays, and mailbox interrupts harness the raw power of 68010 and 68020 MPUs functioning in parallel. This power can be configured to match the most demanding applications.



The Ironics **Performer Series™ UNIX™ Systems** are especially well suited to multi-processor environments. Since all system functions reside on one VMEbus board, UNIX-related bus traffic is completely eliminated. As a debugging tool, UNIX may be used to initiate, monitor, and control the function of a target board set residing on the same backplane. It does this without impacting the target system's use of the bus. UNIX may also function as a front end for multiple processor boards running independent real-time tasks, all under the control and coordination of UNIX.

If you would like to know more about how the Ironics approach to multiprocessing can be used on your next project, write or call for the Ironics ***Multiprocessing Technical Brief.*** Ironics Incorporated, 798 Cascadilla Street, Ithaca, NY 14850, Telephone (607) 277-4060.

Performer Series is a trademark of Ironics Incorporated. UNIX is a trademark of AT&T Bell Laboratories.

IRONICS Incorporated

Circle 4 on reader service card

Electronics
International edition

EDITOR-IN-CHIEF
Robert W. Henkel

EXECUTIVE EDITORS
Samuel Weber (technical), Arthur Erikson (news)

ASSOCIATE MANAGING EDITORS
Howard Wolff, Benjamin A. Mason

ASSISTANT MANAGING EDITORS
Tom Manuel, Jeremy Young

SENIOR EDITOR
Kevin Smith

ART DIRECTOR
Fred Sklenar

DEPARTMENT EDITORS
Business: Robert J. Kozma
Communications: Robert Rosenberg
Computers & Peripherals: Tom Manuel
Government & Military: George Leopold
Industrial & Consumer: David M. Weber
New Products: Steve Zollo, Ann Jacobs
Packaging & Production: Jerry Lyman
Semiconductors: Bernard C. Cole (Palo Alto)
Software & Microsystems: Alexander Wolfe
Test & Measurement: Samuel Weber

NEWS EDITORS
John F. King, Jesse J. Leaf

EDITORIAL PRODUCTION
Charles D. Ciatto (Mgr.), June Noto, Jody LoGrasso

COPY EDITORS
Susan Levi Wallach (Chief), Jay J. Iorio, Bill McIlvaine, Jim Taibi, Sherrie Van Tyle

ART
Sachiko Soskin (Associate Director), Annamaria Palma

NEWS BUREAUS
Boston: Craig D. Rose (Mgr.), Debra Michals
Chicago: Wesley R. Iversen (Mgr.)
Dallas: J. Robert Lineback (Mgr.)
Los Angeles: Larry Waller (Mgr.), Ellie Aguilar
New York: Tobias Naegele (Mgr.)
Palo Alto: Clifford Barney (Mgr.), Denise Caruso, Eve Bennett
Washington: George Leopold
Frankfurt: John Gosch (Mgr.)
London: Kevin Smith (Mgr.)
Paris: Robert T. Gallagher (Mgr.)
Tokyo: Charles L. Cohen (Mgr.), Mari Matsushita, Michael Berger (World News Chief), Jonathan Joseph

EDITORIAL ADMINISTRATION
Denise Giaimo (Administrative Assistant), Laura Aspery, Ina Gruber, Josephine Ortiz

PUBLISHER
Laurence Altman

DIRECTOR OF OPERATIONS
Thomas E. Vachon
CIRCULATION MANAGER
Leon Irgang
PRODUCTION DIRECTOR
Thomas Egan
RESEARCH MANAGER
Elda Vale
CUSTOMER SERVICE MANAGER
Linda Tamburello

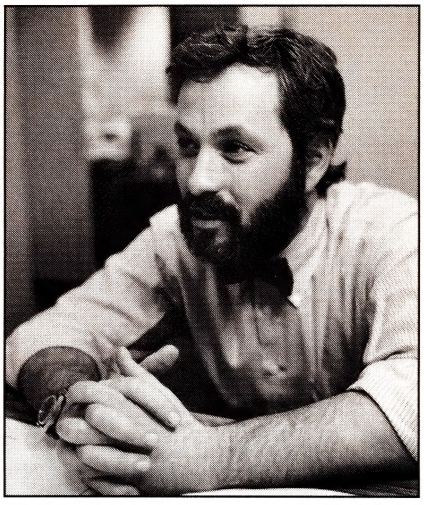
The referee for this week's Battle of the Buses is Bob Rosenberg, who is eminently qualified to write about buses—and to serve as the third man in the ring when the market's competitors meet for the championship.

"When I came to *Electronics* almost two years ago, the first article I handled was on the very same subject," recalls Bob. "But I was a tyro, and the article was written by three authors from three companies making VMEbuses who had never seen each other's products. My job was to take the piece and weave it into a fine mesh. That was some baptism by fire."

Things have changed. "This time it was easier," continues *Electronics*' communications editor, "if for no other reason than the different types of buses have been out there a while, and there is no longer a need to put together a tutorial article. The reader no longer wants to know the merits of synchronous versus asynchronous buses, or message-passing protocols. Now, the question is about available support."

The answers are on p. 48.

Being an art director means one must have a sharp eye, a creative mind, the ability to communicate—and know where to buy boxing gloves. Fred Sklenar can do all those things and more—for 16 years, his illustrations have been making our covers come alive, and his drawings inside the magazine have added color and vitality to these pages. His ability to translate words into graphic concepts is among the best in the business.



ON THE BUS. Rosenberg sizes up the battle.

Still, some translations are easier than others. Take this week's cover for example. The concept, like most good ones, is simplicity itself: a referee declaring that one contestant has won the Battle of the Buses. But the problem was where to find a pair of boxing gloves to photograph.

"You would think that in a city like New York that would be easy," says Fred. "However, most of those in the stores are cheap imitations and would look like that on the cover." The solution? Where else but Madison Square Garden, boxing's old stomping ground, where a sporting-goods store off the lobby had the real thing.

So now *Electronics* magazine has a strikingly graphic cover—and a pair of $60 Everlast gloves.

Laurence Altman

November 25, 1985 Volume 58, Number 47
100,017 copies of this issue printed

Electronics (ISSN 0883-4989). Published weekly by McGraw-Hill Inc. Founder: James H. McGraw 1860-1948. Publication office: 1221 Avenue of the Americas, N. Y., N. Y. 10020; second class postage paid at New York, New York and additional mailing offices. Postage paid at Montreal, P. Q. Registration Number 9034.

Executive, editorial, circulation, and advertising addresses: Electronics, McGraw-Hill Building, 1221 Avenue of the Americas, New York, N.Y. 10020. Telephone (212) 512-2000. Teletype 12-7960 TWX 710-581-4879. Cable address: M C G R A W H I L L N E W Y O R K.

Subscriptions limited to professional persons with active responsibility in electronics technology. No subscriptions accepted without complete identification of subscriber name, title or job function, company or organization, and product manufactured or services performed. Based on information supplied, the publisher reserves the right to reject nonqualified requests. Subscription rates: the United States and possessions $32 one year, $55 two years, $76 three years; company addresses and company libraries $40 one year, $67 two years, $93 three years; Canada and Mexico $34 one year, $57 two years, $78 three years; Europe $50 one year, $85 two years, $125 three years; Japan, Israel, and Brazil $85 one year, $140 two years, $200 three years; Australia and New Zealand $95 one year, $170 two years, $240 three years, including air freight; all other countries $50 one year, $85 two years, $125 three years. Limited quota of subscriptions available at higher-than-basic rate for persons allied to field served. Check with publisher for these rates. Single copies: $3.00. Please allow four to eight weeks for shipment.

Officers of McGraw-Hill Information Systems Company: President: Richard B. Miller; Executive Vice Presidents: Frederick P. Jannot, Construction Information Group; Russell C. White, Computers and Communications Information Group; J. Thomas Ryan, Marketing and International. Senior Vice Presidents: Francis A. Shinal, Controller; Robert C. Violette, Manufacturing and Technology. Senior Vice Presidents and Publishers: Harry L. Brown, Computers and Communications; David J. McGrath, Construction. Group Vice President: Peter B. McCuen, Communications. Vice Presidents: Fred O. Jensen, Planning and Development; Margaret L. Dagner, Human Resources.

Officers of McGraw-Hill Inc.: Harold W. McGraw Jr., Chairman; Joseph L. Dionne, President and Chief Executive Officer; Robert N. Landes, Executive Vice President and Secretary; Walter D. Serwatka, Executive Vice President, Publishing Services; Shel F. Asen, Senior Vice President, Manufacturing; Ralph R. Schulz, Senior Vice President, Editorial; George R. Elsinger, Vice President, Circulation; Ralph J. Webb, Vice President and Treasurer.

Title registered in U. S. Patent Office; Copyright 1985 by McGraw-Hill Inc. All rights reserved. The contents of this publication may not be reproduced in whole or in part without the consent of copyright owner.

Where necessary, permission is granted by the copyright owner for libraries and others registered with the Copyright Clearance Center (CCC), 21 Congress Street, Salem, Mass. 01970, to photocopy any article herein for the base fee of $0.50 per copy of the article plus $0.25 per page. Payment should be sent directly to the CCC. Copying done for other than personal or internal reference use without the express permission of McGraw-Hill is prohibited. Requests for special permission or bulk orders should be addressed to the publisher. ISSN 0883-4989/85 $0.50+.25.

Subscribers: The publisher, upon written request to our New York office from any subscriber, agrees to refund that part of the subscription price applying to copies not yet mailed. Please send change-of-address notices or complaints to Fulfillment Manager; subscription orders to Circulation Manager, Electronics, at address below. Change-of-address notices should provide old as well as new address, including zip codes. Attach address label from recent issue. Allow one month for change to become effective. Subscriber Service: call (201) 356-7980, 9 a.m. to 4 p.m. EST. Postmaster: Please send address changes to Electronics, att. Fulfillment Manager, CN 808, Martinsville, N. J. 08836.

Editorial department phones: Administration (212) 512-2645, News and New Products (212) 512-2685, Technology (212) 512-2666. Bureaus: Boston (617) 262-1160, Chicago (312) 751-3811, Dallas (214) 458-2400, Los Angeles (213) 480-5234, New York (212) 512-6985, San Francisco/Palo Alto (415) 968-2712, Washington (202) 463-1650, Frankfurt 72-5566, London 493-1451, Paris 720-2070, Tokyo 581-9816. **Business departments:** (212) 512-3469 (Business departments follow the Advertisers' Index).

THE FIRST PRACTICAL NON-VON NEUMANN COMPUTER IN FULL SWING.

NEC's NEDIPS—NEC Data-Flow Image Processing System—the world's first practical non-Von Neumann computer is performing well at a remote sensing technology institute in Tokyo.

NEDIPS was originally developed for processing image data from satellite-borne synthetic aperture radar. It has reduced processing time to about 3 hours from over 100 hours required by conventional mainframes.

Our data-flow computer features three advantages over sequential processing. First, system performance is virtually unlimited by memory input/output speed. Instructions are executed in parallel automatically. Programming and debugging are easy because it adopts a functional language.

NEDIPS, with a minicomputer like NEC's MS serving as a host computer, consists of an efficient data-flow processor and memory subsystem which is expandable to 64 Mbytes. Maximum processing speed is 159 MFLOPS. Superior speed and programming ease make the system highly suitable for diverse scientific calculations such as dynamics simulation and differential equations, signal processing and general image processing.

NUMBER 133

V20/V30 FEATURE EXTENSIVE CMOS PERIPHERALS.

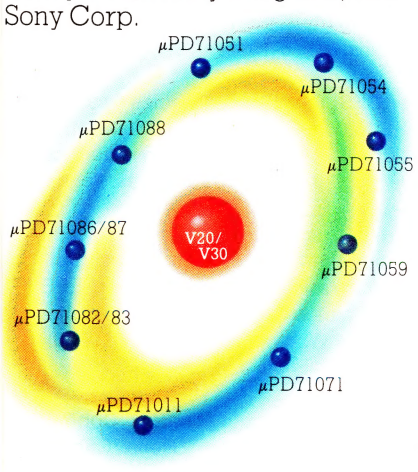
The first 16-bit members of NEC's V-Series CMOS microprocessor family are available with CMOS peripherals. The 8-bit external bus V20 and full 16-bit V30 fit into most existing systems and upgrade performance substantially.

The V20 and V30 feature dual data bus architecture and other hardware refinements to provide outstanding speed. The 101-instruction set includes bit operations, bit field operations, packed decimal operations and stack manipulations. Power consumption rates a low 300mW in operation and 50mW for standby.

Comprehensive CMOS peripherals complement CMOS V20/V30. A CMOS coprocessor (floating point processor) and advanced DMA controller are well under development.

System performance is further boosted with a multi-tasking Real Time OS. Development tools include an In-Circuit Emulator, Relocatable Assembler, Pascal and C compilers.

The V20 and V30 are to be alternately sourced by Zilog Inc., and Sony Corp.



LARGE-CAPACITY INFORMATION DISPLAY PAGER.

The new NEC D4α Information Display Pager packs state-of-the-art technology into a credit card-sized unit weighing only 100 g (3.5 oz).

It receives, displays, and saves a total of 12 messages up to a maximum total of 416 characters. The maximum single message length is 352 characters. Each message appears on the 5 × 7 dot matrix Liquid Crystal Display (LCD), 16 characters at a time. These features enable detailed messages or instructions to be communicated to the IDP user.

Up to eight current messages can be saved and recalled from the PORTAL memory. An additional four important messages can be selectively shifted to the VAULT memory, which protects them from being overwritten.

The two unique addresses assigned to each unit provide both information display and priority tone-only services to the users.

One of four optional alert modes is selectively programmed into each unit. The "Silent Secretary" mode delays received messages until it is convenient for the user to review them. Also, the number of messages received while in this mode will be displayed on the LCD. "Visual Alert", with a blinking red LED, displays and saves incoming messages in memory. "Quiet Alert" sounds a low-level alert tone. "Vibration Alert" blinks the LED and vibrates while it displays and saves incoming messages.

NEC TO SUPPLY FIVE EUTELSAT AND TWO SMS EARTH STATIONS.

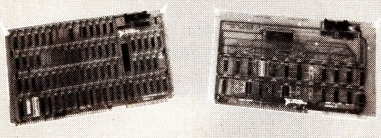
As part of the European Communications Satellite (ECS) System, NEC is supplying earth stations for five member nations of the European Telecommunications Satellite Organization (EUTELSAT). Austria, Portugal, Switzerland and Turkey have ordered complete satellite communications systems, including TDMA/DSI (digital speech interpolation) terminal equipment. NEC has already supplied to Belgium a high-performance 18-meter diameter dish antenna and low-noise amplifier subsystems.

The latest digital technology will be used for telephone transmission to effectively use satellite transponders. The TDMA/DSI system will permit each station to transmit for a fraction of a second using the whole bandwidth of the transponder. The EUTELSAT series of satellites also forms a special network called the Satellite Multi-Service (SMS) System primarily for business users. NEC has also received orders for two SMS and two TV uplink earth stations from Norway.

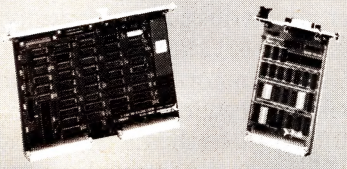
NEC

IEEE-488

MULTIBUS



VMEbus



Interfaces & Software for Multibus & VMEbus

Hardware Flexibility

- High performance applications
  - 500K bytes per second
  - Hitachi HD 68450 LSI DMA controller
- Low cost applications
  - Programmed I/O
  - Multiple IEEE-488 ports per slot
  - Polled or interrupt driven transfers

Software Support

- Real-Time Operating Systems
  - Versados, MTOS
  - PDOS, iRMX
- UNIX

Other IEEE-488 Products

- Interfaces & Software for
  - IBM PC & compatibles
  - DEC Q-bus & UNIBUS
  - STD & S-100 bus
- General GPIB Products
  - GPIB Bus Testers
  - GPIB Bus Extenders
  - Stand-Alone Controllers

NATIONAL INSTRUMENTS

12109 Technology Boulevard
Austin, TX 78727
1 (800 531-GPIB
In Texas (800) IEEE-488
Telex: 756737 NAT INST AUS

MEETINGS

CAIA TO FOCUS ON AI APPLICATIONS

MIAMI BEACH, FLA.

Practical applications, not theory, are a growing interest in artificial-intelligence circles. People are "finding that they can make money" by implementing the technology, says John Roach, general chairman of the Second Conference on Artificial Intelligence Applications.

As evidence, the conference will cover such topics as the growing number of expert-system packages as well as evolving uses of AI in machine vision, robotics, and natural language. Speakers will include Harry Pople, professor of computer science at the University of Pittsburgh, who developed Internist, which has evolved into Caduceus, an expert system for internal-medicine diagnosis (see story, p. 24); B. Chandrasekaran of Ohio State University, known for his AI research into how humans solve problems; and Carnegie-Mellon University's John McDermott, developer of Xcon, an expert system used by Digital Equipment Corp. to configure large-scale computer systems from customer orders.

There is still room for theory, however. Roach, a professor of computer science at Virginia Polytechnic Institute and State University, says natural-language applications software still has limited vocabularies and syntaxes. He says the problem of developing a complete natural-language application is not simply a need for greater machine speed and memory. Technical methods must be discovered to cope with the nuances of human communication.

Work in robotics hasn't quite broken through yet, Roach says. But he predicts that "robotics and vision people will break through in a big way in the 1990s."

1985 Real-Time Systems Symposium, IEEE Computer Society *et al.* (Andre van Tilborg, Computer Science Department, Carnegie-Mellon University, Pittsburgh, Pa. 15213), Sheraton Harbor Island East, San Diego, Dec. 3-5.

WSC '85: Winter Simulation Conference, IEEE *et al.* (Gerard C. Blais, U. S. Air Force, Washington, D. C. 20330), San Francisco Hilton and Tower, Dec. 11-13.

CAIA: Second Conference on Artificial Intelligence Applications, IEEE (Artificial Intelligence, 1730 Massachusetts Ave. N. W., Washington, D. C. 20036), Fontainebleau Hotel, Miami Beach, Fla., Dec. 11-13.

Winter National Design Engineering Show & Conference, Society of Mechanical Engineers (Cahners Exposition Group Inc., 999 Summer St., Stamford, Conn. 06905), Anaheim Convention Center, Anaheim, Calif., Dec. 11-13.

24th IEEE Conference on Decision and Control, IEEE (David S. Spain, Advanced Information & Decision Systems Co., 210 San Antonio Circle, Suite 286, Mountain View, Calif. 94020-1270), Bonaventure Hotel, Fort Lauderdale, Fla., Dec. 11-13.

Expert Systems '85, British Computer Society (Conference Department, BCS, 13 Mansfield St., London, W1M OBP, UK), University of Warwick, London, Dec. 16-19.

1st International Conference on Supercomputing Systems, IEEE (Supercomputing Conference, 1730 Massachusetts Ave., N. W., Washington, D. C. 20036), Innisbrook Resort, Tarpon Springs, Fla., Dec. 16-20.

ATE West '86, Morgan-Grampian Expositions Group (Morgan-Grampian, 1050 Commonwealth Ave., Boston, Mass. 02215), Anaheim Convention Center, Anaheim, Calif., Jan. 6-9.

IC Assembly Automation Conference '86, Society of Automotive Engineers and Integrated Technical Marketing, (Intem, P. O. Box 390207, Mountain View, Calif. 94309), Red Lion Inn, San Jose, Calif., Jan. 8-9.

Hawaii International Conference on System Sciences, University of Hawaii *et al.* (Kim R. Lucak, College of Business Administration, University of Hawaii, 2404 Maile Way, C-202, Honolulu, Hawaii 96822), University of Hawaii, Honolulu, Jan. 8-10.

Business Applications of Approximate Reasoning, Générale de Service Informatique (GSI Services-ARC, 25, Blvd. de l'Amiral Bruix, 75016 Paris, France), Intercontinental Hotel, Paris, Jan. 8-10.

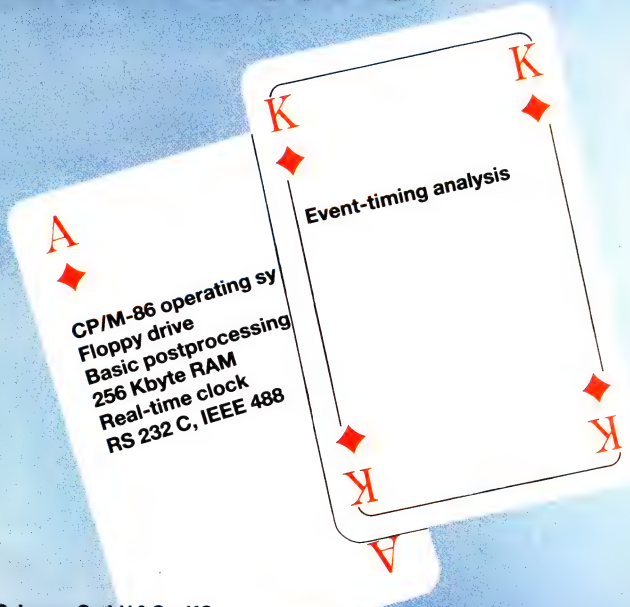
Winter CES, Electronic Industries Association (EIA, 2001 Eye St. N. W., Washington, D. C. 20006), Hilton Hotel, Sahara Hotel, and Las Vegas Convention Center, Las Vegas, Jan. 9-12.

5th Symposium on Reliability in Distributed Software and Database Systems, IEEE (IEEE Computer Society, 1730 Massachusetts Ave. N. W., Washington, D. C. 20036), Los Angeles Marriott, Jan. 13-16.

1986 Winter Usenix Technical Conference, Usenix Association (Usenix Conference Office, P. O. Box 385, Sunset Beach, Calif. 90742), Marriott Hotel-City Center, Denver, Colo., Jan. 15-17.

Logic Analysis System LAS

Full house



With the Logic Analysis System LAS you always have a strong card in your hand. The modular design of the LAS affords optimal configuration for your measurement. The LAS with seven options and μP probes to match all standard microprocessors is counted amongst the best of logic analysis systems.

8-bit μP probes:
8080; 8085/NSC 800; Z80; 6502; 6800/02/08; 6809/09E; 8031/51

16-bit μP probes:
8086/88; 80186/88; 68000

Ethernet test probe

Ask for the detailed brochure **Info LAS**

LAS E 015

Rohde & Schwarz GmbH & Co. KG
Postfach 80 14 69
D-8000 Muenchen 80
Federal Republic of Germany
Telex 523 703 (rus d)
Tel. internat. + (49 89) 41 29-0

ROHDE&SCHWARZ

Circle 80 on reader service card

SIEMENS

Capacitor chips for surface mounting

The tiny ones for modern automatic placement

Capacitor chips merge proven know-how in technology with rationalized methods of assembly.

Siemens now brings you all the benefits of surface mounting with the right SMD capacitors for every application:

- **ceramic chips with excellent RF specs**
- **metalized-plastic-film chips with self-healing dielectric**
- **tantalum chips with low self-inductance**

All are fully qualified for dip and wave soldering. Tight dimensional tolerances guarantee straightforward, automatic assembly.

Capacitances range from 1 pF through 100 µF, with voltage ratings of 6.3 V to 100 V. And the chips come in all conventional forms of packaging.

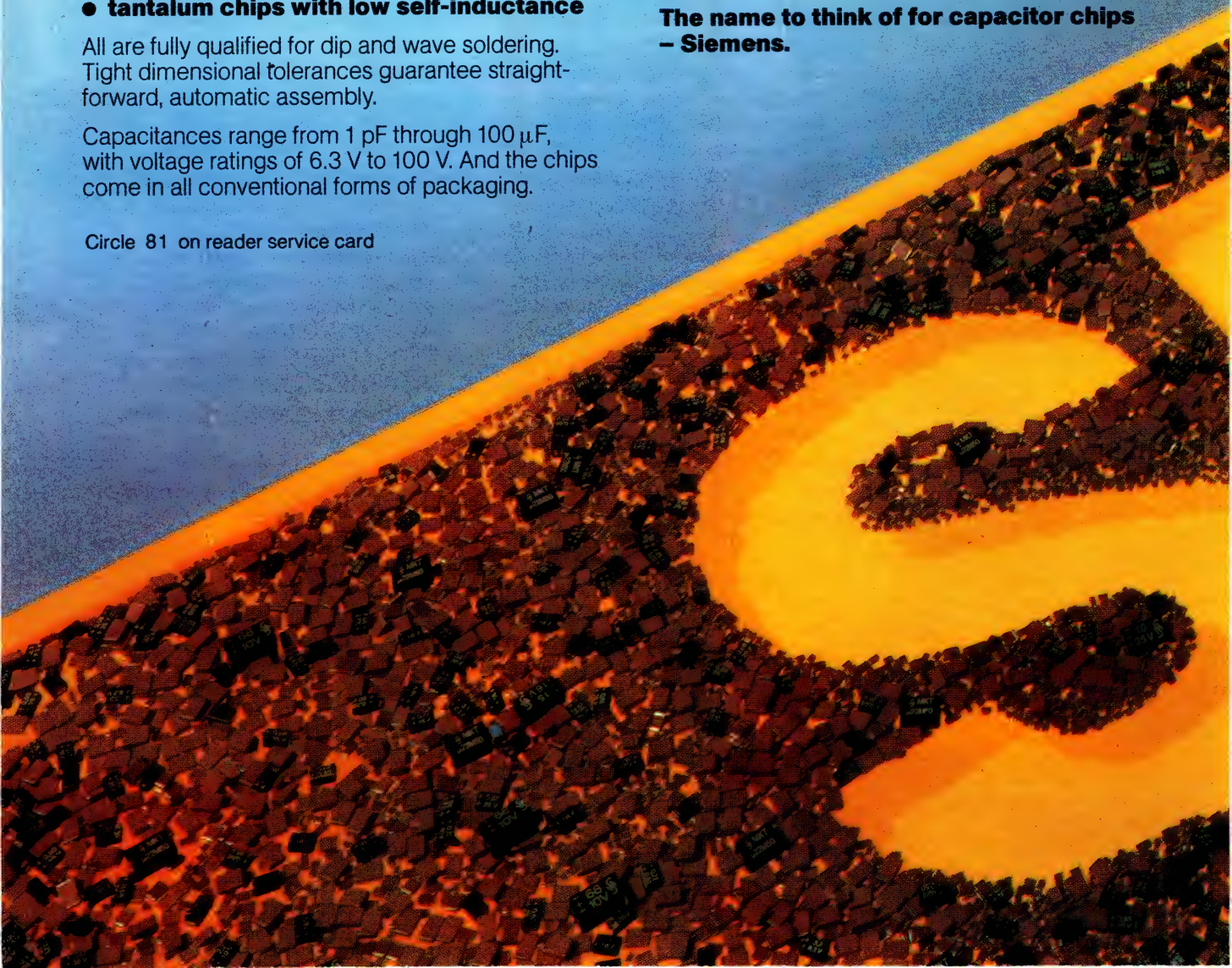
Circle 81 on reader service card

That's not all though, because Siemens is also a specialist in the automatic placement machines that SMDs call for.

Siemens is ahead. Through experience, research and development, innovation. Find out what all this can do for you. Write Siemens AG, Infoservice 12/1172, Postfach 156, D-8510 Fürth, W. Germany, quoting "capacitor chips".

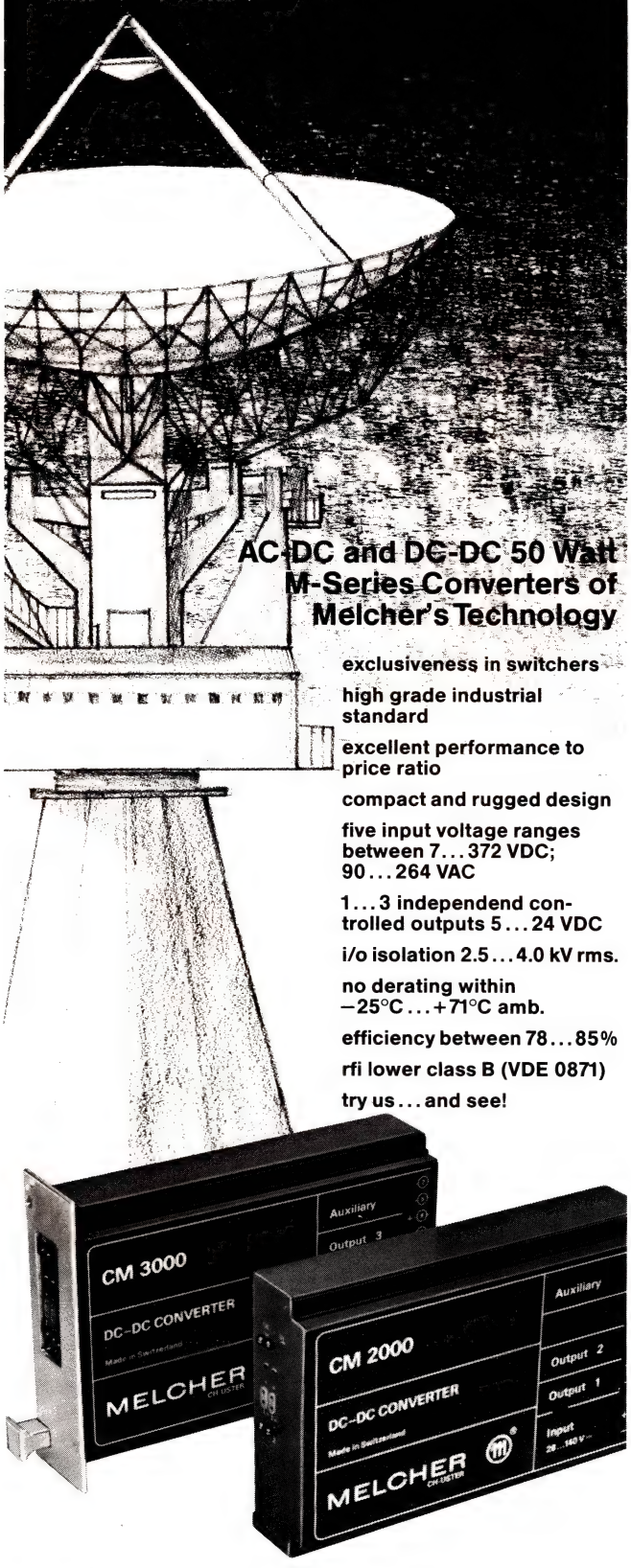
The name to think of for capacitor chips – Siemens.

12/1172-101



MID

Novelty



AC-DC and DC-DC 50 Watt M-Series Converters of Melcher's Technology

- exclusiveness in switchers
- high grade industrial standard
- excellent performance to price ratio
- compact and rugged design
- five input voltage ranges between 7...372 VDC; 90...264 VAC
- 1...3 independend controlled outputs 5...24 VDC
- i/o isolation 2.5...4.0 kV rms.
- no derating within −25°C...+71°C amb.
- efficiency between 78...85%
- rfi lower class B (VDE 0871)
- try us... and see!

CM 3000 DC-DC CONVERTER MELCHER

CM 2000 DC-DC CONVERTER MELCHER

MELCHER®

elektronische Geräte AG

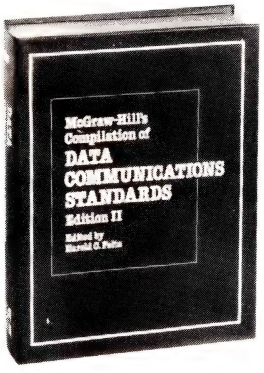
CH-8610 Uster, Switzerland, Tel. 01/941 37 37, Tx 57154 meus ch

4E Circle 82 on reader service card

NEW EDITION

Complete and Unabridged American and International

DATA COMMUNICATIONS STANDARDS



All standards are new, revised, or reaffirmed since the previous edition

1,923 pages
illustrated
Edited by Harold C. Folts

Presents all 123 interface protocol standards set by:
• International Telegraph and Telephone Consultative Committee (CCITT) • International Organization for Standardization (ISO) • European Computer Manufacturers Association (ECMA) • American National Standards Institute (ANSI) • Electronic Industries Association (EIA) • U.S. Government (NBS and NCS)

Special feature for instant access:
Cross-reference tables of the standards of each group corresponding to those published by the others.

An essential reference for all who are exploring, planning, developing, manufacturing, or using data communications equipment or networks.

Return Coupon to:
Data Communications Standards II
Electronics Magazine Books
McGraw-Hill Intl. Publications Co.
European Circulation Center
Maidenhead, Berks. SL6 2QL,UK
(Tel. (0628) 23431; Telex 848640)

Send me _____ copy (copies) of R100-**DATA COMMUNICATIONS STANDARDS EDITION II** at $295. U.S. orders please add local sales tax. McGraw-Hill pays regular shipping and handling charges on prepaid orders. Ten-day money-back guarantee applies.

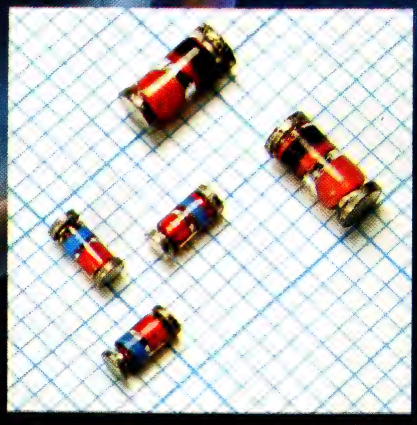
☐ Check enclosed ☐ Bill me ☐ Bill company
☐ Company Purchase Order enclosed.

Name
Title
Company
Address
City
State/Zip (U.S.)
Country (outside U.S.)

ELV

SMD diodes.

The time is ripe for surface mounting. With quality SMDs from ITT Semiconductors.



For instance, SMD diodes in hermetic glass package

You can make the most of surface mounting with SMD diodes from ITT Semiconductors:

- Surface mounting can reduce your production costs by up to 90% at a stroke.
- It will also open the door to more compact end-product design and
- measurably higher reliability.

We offer a wide range of SMD diodes, hermetically sealed in high quality glass packages: tuning diodes, band switching diodes, 500 mW and 1 W Zener diodes, switching diodes, Schottky diodes and universal diodes. Available in MiniMELF and MELF glass packages for superior protection, and supplied either in bulk or in 8 or 12 mm tape packaging.

Our manufacturing capacities are the world's largest. You can rely on ITT Semiconductors for world-wide support and product availability plus up-to-the-minute know-how for all applications.

ITT Semiconductors Benelux, Francis Wellesplein 1, B-2018 Antwerp, Tel. (03) 2381312, Telex 72128
ITT Semiconductors France, 157, rue des Blains, F-92220 Bagneux, Tel. (1) 5478181, Telex 260712
ITT Semiconductors Germany, P.O.Box 840, D-7800 Freiburg, Tel. (0761) 5170, Telex 772715
ITT Semiconductors Iberia, Poligono Industrial, E-45080 Toledo, Tel. (25) 231350, Telex 27707
ITT Semiconductors Italy, Viale Milanofiori, E/5, I-20090 Assago (Mi), Tel. (02) 82470.1, Telex 311351
ITT Semiconductors Japan, P.O.Box 21, Sumitomo Building, Shinjuku-ku, Tokyo 160-91, Tel. (03) 3478881-5, Telex 22858
ITT Semiconductors Scandinavia, Naverland 29, DK-2600 Glostrup, Tel. (02) 451822, Telex 33355
ITT Semiconductors United Kingdom, 145-147 Ewell Road, Surbiton, Surrey KT6 6AW, Tel. (01) 3906577, Telex 928622

ITT Semiconductors

Circle 87 on reader service card

The high-performance, high-density interconnect for today's tighter budgets.

Hardworking Ds, from AMP.

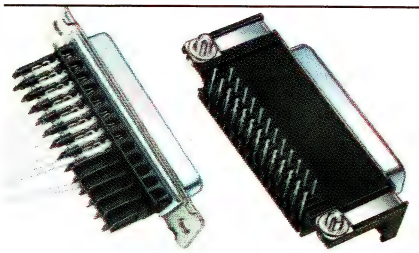
One of the latest additions to this giant family of space-savers offers pre-loaded, insulation-displacement contacts for mass termination.

Save on application costs. And save more with select loading, by paying only for the contacts you intend to use.

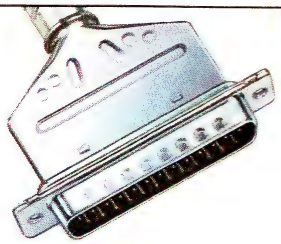
Our Ds also come with a range of shielding options to block EMI/RFI, including full metal cable clamp assemblies or lightweight (and low cost) metalized plastic housings. We even offer a snap-together "generic" shell designed to allow postmolding your own housing.

Other D-lights? Our high-density Commercial 90 Series uses a smaller-size contact, to pack more circuits in. And we offer our MIL-series coax and power contacts in a broad range of configurations, to pack more functions in as well.

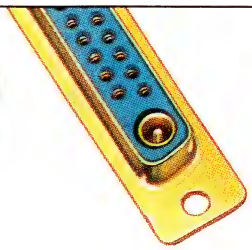
Find out now how selection, performance, and total economy can help you keep your budget in trim. Give us a call.



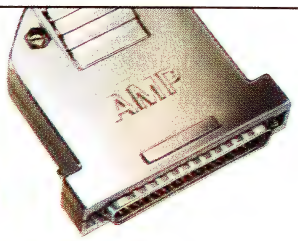
Our select-loaded, insulation-displacement RS 232 style—with the recently introduced board mount with grounding strap, 440 threaded inserts, and board locks.



Snap-together metal shields block EMI, allow you to postmold your own housings.



Our MIL-version subminiature Ds come with optional power and coax contacts, in a variety of configurations.



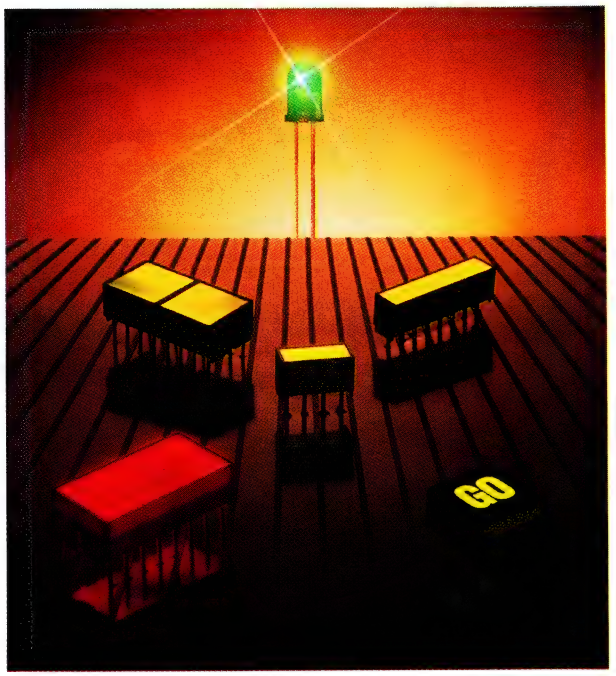
AMP Commercial 90 connectors, through the use of smaller pin-and-socket contacts, offer almost double the density of standard Ds.

Call (717) 780-4400 and ask for the AMPLIMITE Connector Desk. AMP Incorporated, Harrisburg, PA 17105.

AMP Interconnecting ideas

AMP and AMPLIMITE are trademarks of AMP Incorporated.

Light up your legends.



Light bars.

Intense, even areas of light. Thin enough to fit into most any design.

Stackable.

A perfect backlight. A light source for your annunciators.

So convenient you're finding them in automotive panels, computer peripherals, appliances, instrumentation and industrial controls.

The LightHouse is now a major supplier of light bars. Our family consists of the five most popular packages. Each comes in three high intensity colors–red, yellow and green.

These are industry standard products that have the exact pin, package and function as light bars currently in use. In fact, our products and HP's share the same part numbers.

The convenience of light bars

Before light bars you had only two alternatives: a custom house or doing your own design. The first solution was expensive, the other a royal pain.

General Instrument gives you a pre-engineered device with no hot spots. Luminescence is the most uniform in the industry, especially in large light bars. And our binning scheme produces tighter, more aesthetic matching.

Remember, think LightHouse.

Whenever you want to see your name in lights.

General Instrument light bars are available from Arrow, Hamilton/Avnet, Kierulff, Schweber and Wyle. Or write for our data sheets. For samples please send your request on letterhead.

PART NO.	DESCRIPTION	PACKAGE
HLMP-2300 HLMP-2400 HLMP-2500	2 LED Single-in-line 0.35 in. x 0.15 in. Area	A
HLMP-2350 HLMP-2450 HLMP-2550	4 LED Single-in-line 0.75 in. x 0.15 in. Area	B
HLMP-2655 HLMP-2755 HLMP-2855	4 LED Dual-in-line 0.35 in. x 0.35 in. Area	C
HLMP-2670 HLMP-2770 HLMP-2870	Dual 0.35 in. x 0.35 in. Area Dual-in-line package	D
HLMP-2685 HLMP-2785 HLMP-2885	8 LED 0.35 in. x 0.75 in. Area Dual-in-line package	E

General Instrument, Optoelectronics Division, 3400 Hillview Avenue, Palo Alto, CA 94304. Phone: (415) 493-0400. TWX/TLX: 470208.

GENERAL INSTRUMENT
Optoelectronics Division

The LightHouse you can depend on.

TECHNOLOGY NEWSLETTER

TOSHIBA'S HEMT DEVICE WILL FOLLOW GOULD'S TO MARKET

Gould Inc. is the first to market with a high-electron-mobility-transistor product, but it won't be alone for long. Toshiba Corp., for one, expects to start selling a more advanced device next year. If the superfast devices catch on, other semiconductor makers figure to join the fray. Gould's aluminum gallium arsenide-GaAs device, the H503, is intended mainly for satellite, radar, and electronic warfare systems. At 18 GHz, the new HEMT shows a gain of 9.5 dB, 2 dB more than the GaAs FET it supplants. The noise figure is improved as well: 1.8 dB, compared with 2.2 dB. The Rolling Meadows, Ill., firm uses standard 0.5-μm minimum geometries for the H503 and expects to get down to geometries close to 0.25-μm later. Toshiba is already there with its S8900 HEMT. Fabricated with 0.25-μm gate lengths, the S8900 boasts an ultralow noise figure of 1.3 dB at a gain of 9.5 dB at 18 MHz. At 30 MHz, these parameters are a noise figure of 2.4 dB and a gain of 7.5 dB. □

3M AND OPTIMEM TEAM UP ON OPTICAL-DISK DRIVE

Volume production of 5¼-in. optical-disk drives that can read, write, and erase on all types of optical media will come within two years, claim 3M Corp. and Optimem, a Sunnyvale, Calif., subsidiary of Xerox Corp. The two announced a technology agreement at last week's Comdex/Fall '85 in Las Vegas. The Minneapolis company will manufacture an erasable medium—the first plastic, pregrooved, preformatted substrate available—starting in January. Optimem, a maker of write-once drives, is responsible for the hardware design: a magneto-optic read/write mechanism that can work with other types of media as well. □

GE BRINGS SMART-POWER TECHNOLOGY TO ASIC MARKET

General Electric Co. intends to bring new power to the market for application-specific integrated circuits. The company's Semiconductor Business Division, Syracuse, N. Y., has opened up its proprietary smart-power technology, called GE-Smart, so its customers can add power devices to their ASICs. GE's mixed process includes junction-isolated analog and digital elements that can be combined for a wide variety of circuit building blocks with ratings up to 500 V. The circuits can be designed as fully integrated chips or—for lower cost—hybrid circuits in plastic or ceramic packages. GE will also offer standard products designed with the technology. The first, the GE1E10MA, is a control circuit for fractional-horsepower electric motors, rated at 500 V and able to switch up to 10 A in less than 1 μs. □

RADIO PAGERS MONITOR INSTRUMENTS REMOTELY

Process Automation & Computer Systems Ltd., a startup in Southampton, England, hopes to make instrumentation cabling at industrial sites a thing of the past with a novel radiotelemetry system. The Pacslink system scans up to 450 instruments every 30 seconds over a single radio channel, rated at 1- to 2-mW radiated power at a frequency of 150 to 200 MHz (400 MHz in the U. S.). The link operates at 2 kb/s, but an eight-level security code, needed to guarantee a data integrity of less than one false message in 200,000 years, cuts the useful data rate to 125 b/s. Battery-powered slave units are based on a single-chip radio pager developed by STC Telecommunications Ltd.'s Defence Systems Division [*Electronics,* Aug. 12, 1985, p. 20]. Separate STD-bus boards are used for the transmit/receive module, microprocessor, and interface, allowing a building-block approach for systems. The company says its gear could save $1 million in cabling for a new site, and new instruments can be readily retrofitted at existing sites. □

The Sooner You Face Up To Your Faults The Better.

The faulty component that costs you 50¢ to find at incoming inspection, could cost you $5 on the board, $50 in the system, and $500 to repair in the field.

Clearly, the way to minimize test costs and maximize yield is to face up to your faults as they come through the door.

GenRad's broad line of component ATE can help you in this task.

Our 173X family handles digital, memory, and linear devices. And our huge library of test programs gives you fault coverage no other vendor can match.

And then there's SCAN™, the first test data management software for incoming inspection. SCAN gives you real-time process feedback to help you evaluate vendors and formulate test strategies.

So for cost-effective ATE, think of GenRad first.

Because the most costly faults are the ones you find out about last.

Call 1-800-4-GENRAD, or write GenRad, 170 Tracer Lane, MS32, Waltham, MA 02254.

GenRad®

© GenRad, Inc., 1985. SCAN is a trademark of GenRad, Inc.

ELECTRONICS NEWSLETTER

JAPAN'S MEMORY MAKERS FACE HARD TIMES

Evidence is surfacing that Japanese memory makers have run into hard times as a result of the steep market slide in the U. S. Total Japanese memory inventories are approaching $1 billion, estimates market watcher Jack Beedle of In-Stat Inc. This level is far above the 0.4 : 1 ratio, measured against annual production, that most companies seek. Among those cutting back production is sales leader NEC Corp., which was building 64-K random-access memories at a monthly rate of 12 million in January. It now expects to be building 1 million a month by year end, with some three to five months' worth in inventory. Industrywide, the Japanese will use only about 65% of MOS capacity during 1985, says Integrated Circuit Engineering Corp., a consulting company in Scottsdale, Ariz. Nonetheless, Japanese capacity has more than doubled since 1983. □

AT&T PUTS ITS WEIGHT BEHIND VMEBUS STANDARD

AT&T Information Systems joined the VMEbus camp by announcing at Wescon that it would market a 32-bit single-board computer, supporting its latest version of Unix, for the widely used bus. The board contains an AT&T 32100 microprocessor—which operates at 18 MHz—as well as math-acceleration and memory-management chips, 1 megabyte of dynamic random-access memory, and the logic interface for the VMEbus. AT&T said it chose the VMEbus for its first single-board computer product because the bus's specifications are stable and it enjoys the support of some 200 vendors worldwide. However, AT&T will develop an interface for Intel Corp.'s Multibus if market conditions demand it, a representative says. □

MOTOROLA TO REPLACE MASK ROMs WITH EPROMS

Motorola Inc. is taking the mask off high-density read-only memories. MOS-memory officials in Austin, Texas, say the 256-K ROM will be Motorola's last generation of commodity mask-programmed memories. Higher densities will be served with CMOS ultraviolet-erasable programmable ROMs. To drive prices down to the ROM range, one-time programmable EPROMs will come in windowless plastic packages, says John Barnes, director of memory design. In large volumes, however, mask ROMs will still be offered as custom parts. Motorola will keep its n-MOS version of 256-K ROM on the market, but the company has phased out its CMOS design [*Electronics*, June 30, 1982, p. 81]. The multistate ROM saved silicon but it was too slow for today's computer markets—the task of sensing four currents from the multistate array resulted in a 300-ns maximum access time. Now look for Motorola to replace the part with a CMOS one-time programmable 256-K EPROM. □

AEA LOOKS TO ADD CLOUT IN WASHINGTON

The American Electronics Association is sending out a clear signal that it intends to flex its muscles in Washington by selecting a veteran executive of the procurement wars as its new president and chief executive officer. J. Richard Iverson, senior vice president for government marketing at Gould Inc., was named last week to succeed E. E. Ferrey as chief of the 2,800-member trade association. He'll take office Jan. 1, and his term runs one year. Iverson, who oversaw Gould's half-billion-dollar government sales, also has extensive manufacturing experience and at one time was San Diego chairman of the AEA's predecessor, the Western Electronic Manufacturers Association. He lists taxes, trade, and procurement as the AEA's prime concerns in Washington. "The electronics industry is the nation's biggest," he notes. "But it has been slow in exercising its strength with the federal government." □

Uplifting news.

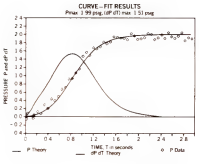
Now we've got application software to support our data acquisition hardware for the IBM PC.™

Hold up a minute!

Now you can get all your analog I/O application software at the same place you get your IBM PC compatible hardware. Data Translation.™

We've got four application software packages that cover a broad range of capabilities, all compatible with the DT2801 series of seven analog I/O boards. So you'll never have to write a line of code again.

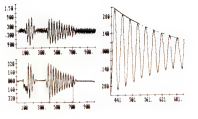
Take a look at these:



Graph Using Curve-Fit

DT/NOTEBOOK

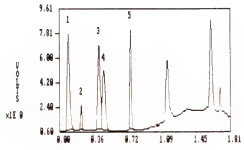
For the non-programmer. An easy-to-use menu-driven package for real-time data acquisition, process control, and data analysis that automatically interfaces to spreadsheet packages. Its menu-driven interface is ideal for users who aren't very familiar with computers.



Analysis Functions with Multiple Window Display

ASYST

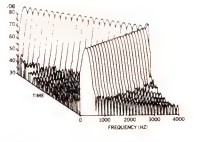
For the advanced user. A command-driven package for real-time data acquisition and control, advanced data analysis, and graphics display. For the user who requires more sophisticated graphics and analysis capabilities.



Peak Detection and Integration

CHROMLAB

For the chromatography scientist. A menu-driven, scientific software package for chromatography and spectroscopy applications. For users who need to do real-time data collection/display, peak detection/integration, and report generation.



3-D Spectral Display

DT/ILS–PC 1

For the signal processing scientist. Command-driven software for digital signal processing that supports data acquisition, waveform manipulation, design and use of digital filters, and spectral analysis. For users who need advanced analysis tools in both time and frequency domains.

* * *

Call us today. We'll help you choose the right package to give your data acquisition the boost it needs.

Fred Molinari, President

Call for our new 576 pg. catalog/ handbook or see it in Gold Book 1985.

Call (617) 481-3700

DATA TRANSLATION

World Headquarters: Data Translation, Inc., 100 Locke Dr., Marlboro, MA 01752 (617) 481-3700 Tlx 951 646
European Headquarters: Data Translation, Ltd., 13 The Business Centre, Molly Millars Lane, Wokingham Berks, RG112QZ, England Tlx 851849862 (#D)
International Sales Offices: Australia (61) 2-6635289; Belgium (32) 2-7352135; Canada (416) 625-1907; Chile (2) 2-253689; China (408) 727-8222, (86) 87214017; Denmark (02) 187188; England (44) 0734-793838; Finland (358) 0-372-144; France (33) 146306839; Greece (30) 031-527039, (30) 13-614300; Hong Kong (852) 3-324563; India (91) 2-231040; Israel (972) 3-324298; Italy (39) 2349751; Japan (81) 3-502-5550, (81) 3-348-8301, (81) 3-355-1111; Korea (82) 753-3101; Malaysia (60) 3-36299; Morocco (21) 9-30-6949; Netherlands (31) 70996360; New Zealand (61) 2-663-5289; Norway (47) (02) 559050; Peru (51) (14) 31-8060; Philippines 818-0103, 818-3073, 818-4230; Portugal (351) 1545313; Singapore (65) 271-3163; South Africa (27) 12469221; Spain (34) 14558112; Sweden (46) 87617820; Switzerland (41) 17231410, (41) 22360830; Taiwan (86) 2-721-7864, (86) 2-531-2434; West Germany (49) 89809020.

DT/NOTEBOOK © 1984, Laboratory Technology Corp. ASYST © 1984 Macmillan Software Co. CHROMLAB © 1984, University of Southern California. DT/ILS-PC 1 © 1984, Signal Technology Inc. IBM is a registered trademark of IBM Corp. Data Translation is a registered trademark of Data Translation, Inc.

PRODUCTS NEWSLETTER

NEW DEC PDP-11 TOPS THE LINE

Digital Equipment Corp. says its MicroPDP-11/83 raises the MicroPDP-11 family's performance to a new height, thanks to an 18-MHz chip set—the J-11 microprocessor and a floating-point accelerator—and a high-speed data path between processor and memory. Current MicroPDP-11s do not use the floating-point accelerator. The new system is comparable in performance to the PDP-11/70 minicomputer, rated at just under 1 million instructions/s for single-precision floating-point operations. The Maynard, Mass., company says the system protects users' huge software investments by running all programs written for older PDP-11 computers. Prices start at $34,360. □

DESPITE THE ODDS, TI STEPS UP DRAM ACTIVITIES

Texas Instruments Inc. is stepping up its thrust in dynamic RAMs, even as other U. S. semiconductor makers back away from the no-longer-profitable market. TI's wholly owned subsidiary in Japan says it will soon supply two organizations of its 1-Mb design, configured as 1,024-K by 1 bit and 256-K by 4 bits. The by-1-bit chip is expected to be available in five versions: page mode; three nibble modes, 4-bit, 8-bit, and extended; and a static-column-decode mode. The 1-μm CMOS parts have access speeds of 100, 120, and 150 ns. TI is delivering samples to major customers now and expects to put parts on the market in early 1986. Prices have not been set. □

SUPERMINICOMPUTER EXECUTES 20 MIPS

A new version of Integrated Digital Products Corp.'s high-speed superminicomputer, the Whetstone II, executes 20 million instructions/s, a 50% increase over the previous model. The Anaheim, Calif., company credits very large-scale integration and a reduced-instruction-set-computer architecture with the increased speed. In the Whetstone II, the 16-bit ECL-based CPU that previously required a full board has been packed onto a single chip. Instructions execute in 50 ns. Priced at $21,000 each, the Whetstone II can be delivered in 30 days. □

PRO-LOG TURNS IBM PC INTO A FACTORY WORKER

Pro-Log Corp. is adapting the IBM Personal Computer architecture to the STD bus that is widely used in factory-control applications. The Monterey, Calif., company's STD-DOS system, shown at Wescon last week in San Francisco, includes an 8088 CPU card that runs under the DOS operating system. Application programs can make DOS calls to RAM that emulates disks. STD-DOS contains 256-K bytes of ROM, 512-K bytes of RAM, and 128-K bytes of battery-backed RAM configured to emulate three disks. The $1,690 basic system will be available in January. □

LSI LOGIC COMBINES ARRAYS AND STANDARD CELLS

LSI Logic Corp. marked last week's Wescon show with the introduction of what it calls composable arrays: a method of semicustom design combining features of gate arrays and standard cells. At the same time, the San Jose, Calif., company introduced the first elements in its LST20 family of standard cells and its LSC20 family of larger megacell-like building blocks, which it calls structured cells. Customers using composable arrays would use the LST20 and LSC20 series to design a master slice similar to LSI Logic's structured arrays. This slice would include a gate array that allows the part to be customized. The LST20 and LSC20 families are fabricated with a 2-μm two-level-metal CMOS process. □

Electronics

BEHIND MOTOROLA'S SILENCE: AMBITIOUS PRODUCT PLANS

COMPANY UNWRAPS A SLEW OF PRODUCTS, COMMITS TO BiMOS

PHOENIX, ARIZ.

During the severe industry slide of the past 18 months, Motorola Inc.'s Semiconductor Products Sector adopted an extremely low profile, with very few meetings, announcements, or interviews. But evidently the company kept up a frenetic pace behind the scenes. The undiminished research and capital spending could well pay off: Motorola officials earlier this month rolled out ambitious plans for next year.

The flood of improvements in products and technology, in a period when many competitors are tapering off, caught Motorola watchers by surprise.

What stood out in the outpouring of announcements was Motorola's commitment to lead the way in BiMOS technology. Though BiMOS chips are tricky to build because they combine somewhat incompatible bipolar and CMOS processes, the chips are very much in demand for their advantages (see "BiMOS technology is worth the effort," below). Motorola, which has worked on BiMOS since the early 1980s, plans to apply it across all product lines.

BiMOS ARRAYS. With its first BiMOS product, the new MCA6000ETL Macrocell, Motorola has what it believes is the only BiMOS gate array. The 6,000-gate circuit is now at the sampling stage for prospective customers and will be in volume production in the first quarter of 1986, say company officials. Furthermore, a roster of BiMOS devices will follow during 1986, including a 1.5-μm 4-K random-access memory.

In the 32-bit microprocessor arena, Motorola has two major speed upgrades in the works for its 68020 microprocessor: a 20-MHz version is due next month and a 25-MHz part next year. At present, 68020s run at 12.5 and 16.67 MHz. The company has shipped about 50,000 32-bit chips this year.

One factor pushing advanced commercial chips to market is the Defense Department's Very High-Speed Integrated Circuits program, say Motorola officials. The VHSIC program's fallout advantage was previously not taken seriously by many in the industry, but it has lately given signs of becoming important [*Electronics*, Nov. 4, 1985, p. 18].

Motorola is more than matching VHSIC funding on its own, but gives such spending credit for providing the test bed for developing high-yield high-volume manufacturing technology for a commercial thrust. Accordingly, it sees a competitive edge for the company in being the only major semiconductor maker to play a role in both VHSIC's 1.25-μm Phase 1 and 0.5-μm Phase 2.

ENTHUSIASTIC. Motorola's Tooker is ready to boast about a host of new products.

Future Motorola work in dynamic-RAM technology will center entirely on CMOS technology. A 256-K chip is scheduled for sampling early next year, while the first 1-Mb chip will go into initial processing during the first quarter. The company is dropping its 256-K n-MOS DRAM, citing predatory pricing and dumping by Japanese suppliers [*Electronics*, Nov. 18, 1985, p. 19].

Motorola's ambitious plans came to light earlier this month at a briefing for the industry press, financial analysts, and market consultants. The official position was that Motorola's policy was to keep quiet about operations while the IC business stayed in the dumps. "That products were kept under the bushel basket is probably our fault," said Gary L. Tooker, corporate executive vice president and sector general manager.

Observers were impressed by the scope of improvements throughout every product line. "I'm amazed by the breadth," says Jack Beedle, a consultant at In-Stat Inc., Scottsdale, Ariz. "Also, the presentation was upbeat, with nothing negative about the Japanese."

But officials did not downplay how hard the continuing semiconductor recession has hit the company and did not predict an imminent upswing. Assistant general manager James Norling noted that the company cut its work force by some 9,000 employees from the 1984 peak. Although Motorola does not re-

BiMOS TECHNOLOGY IS WORTH THE EFFORT

Motorola Inc., which has been exploring BiMOS technology for about five years, revealed plans in mid-November to apply it across a wide range of products. BiMOS combines the low-power and high-noise margins of CMOS with the switching speed and current drive of bipolar. In theory, with BiMOS technology the processes can be adjusted to accentuate the advantages most needed by an application.

As with most mixed-technology chips, however, putting circuits together has caused design and production problems. Incompatibility of processes is especially evident with BiMOS, say consultants, because CMOS chips generally have a horizontal layout, which is difficult to mesh smoothly with the vertically oriented bipolar structures.

The two leaders in BiMOS work are Motorola and Hitachi Ltd., with the Japanese company thought to be somewhat ahead, at least until Motorola announced a 6,000-gate array earlier this month. This development could boost Motorola's standing, says consultant Will Strauss of Forward Concepts Inc., Scottsdale, Ariz. "It's unique and could give them a leg up." First users would likely include manufacturers of high-performance computers. *–L. W.*

port semiconductor results by quarter, financial analysts at the briefing estimated that losses for the third quarter exceeded $50 million.

Despite pressure on sales and profits, Motorola "is gaining market share in all segments except MOS memories," says Charles Thompson, senior vice president and director of world marketing. He predicts that final results for 1985 will show Motorola nearly tied for leadership in world sales with Texas Instruments, NEC, and Hitachi.

The company has not cut back appreciably on capital spending, which totaled $411 million for 1984 or on research. Norling named three production areas slated for the lion's share of next year's spending: further development of the HCMOS (Motorola's high-performance CMOS process) lines, which will make up 75% of microprocessor production in 1987; surface-mount packaging; and a power-device line that Motorola calls TMOS.

Among the other new products announced, most of them for introduction in 1986, were:

- Motorola's first single-chip 16-bit microcomputer, the 68HC16, combining a microprocessor and controller, a competitor of the Intel 8096.
- A one-chip Winchester disk-drive controller that can be mounted on the drive itself, replacing an entire board.
- An electrically erasable programmable read-only memory for military and automotive customers, Motorola's first product in this market in five years.
- The MC13020 "C-Quam" demodulator chip for AM stereo systems.
- Some 13 new chips for the data-communications and telecommunications markets.

–Larry Waller

SIA URGES REFORM OF MILITARY PROCUREMENT

The movement to reform procurement of semiconductors for military systems has gained momentum from the Semiconductor Industry Association. The SIA recently proposed the formation of a joint government-industry board that would encourage the use of current circuit technology and quality-control methods. SIA officials say the board would include representatives from the Defense Department as well as from the ranks of the semiconductor industry and government contractors.

The proposal was made at a mid-November meeting in Arlington, Va., between members of the SIA's Government Procurement Committee and procurement officials representing the Pentagon, the Commerce Department, and other executive-branch agencies. The SIA formed the committee in March to address growing government procurement problems, such as testing and the diminishing sources of components for weapons systems [*Electronics*, Oct. 14, 1985, p. 42].

Along with proposing the joint board, the SIA committee advocated replacing the number of source-control drawings needed for military systems with a standardized two-page procurement specification. Several government officials indicated at a press briefing later that they would at least go along with the SIA plan to form a board.

During the closed meeting, Anthony B. Holbrook, executive vice president and chief operating officer of Advanced Micro Devices Inc., explained the SIA's reasoning to government officials. "Under current procurement practices, semiconductor manufacturers find it difficult to provide the government with the latest technology, to ensure the highest standards of quality and reliability, and to provide components at the lowest cost consistent with meeting the first two objectives." The proposed board would "establish basic policies and objectives for the improvement of the current government semiconductor procurement system," he said.

"We feel there is a very strong need for standardization in specifications and products," says Jon E. Cornell, a senior vice president with Harris Corp. and chairman of the SIA committee. He says there is little room to incorporate into the military sector advances such as statistical quality controls that are now standard in the commercial sector. One reason, the SIA argues, is that the government specification system makes it difficult for chip makers to achieve the production volumes necessary to use statistical controls and minimize costs.

"We have no problems with the establishment of a high-level management board," says Darrell Hill, chief of the Defense Electronics Supply Center's microcircuit qualification branch. But Hill, who represented DESC at the SIA meeting, does take issue with the proposed two-page procurement specifications.

"We don't think it's adequate" to ensure quality and reliability, he says. "We feel that you need a full DESC drawing." Hill further maintains that current military specifications already encourage the use of available circuit technology along with statistical quality controls.

–George Leopold

COMPUTERS

GOING FOR THE 60-GIGAFLOPS MACHINE

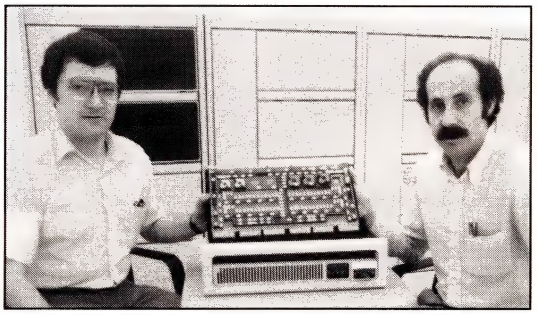
PRINCETON, N. J.

Bypassing global communication in favor of a fast local link and squeezing extra speed out of commercial microprocessors has enabled Princeton University researchers to build a parallel-processing supercomputer that they say cranks out 400 million floating-point operations per second per node. The team envisions a 128-node system that would hit peak speeds of about 60 gigaflops [*Electronics*, Nov. 18, 1985, p. 17].

The machine, now taking shape under the direction of Daniel M. Nosenchuck and funded by the National Aeronautics and Space Administration, uses a fast three-dimensional switch to connect massive amounts of memory with an array of floating-point processors in each node. Data can be fetched from a neighboring node as fast as it can be requested through the switch.

The node-connection architecture is a subset of the California Institute of Technology's Cosmic Cube [*Electronics-Week*, Oct. 8, 1984, p. 29], which links each node to some of its neighbors. But whereas most Cube designers wrestle with the problem of linking many medium-performance nodes, Nosenchuck's aim was the most powerful nodes he could build. He did this by selecting fast available components and by making local data paths as wide as possible.

Each node in the Princeton computer has 24 Advanced Micro Devices Inc. 32-bit emitter-coupled-logic microprocessors and up to 2 gigabytes of memory. All but two of the processors are Am29325 floating-point units, which usually operate at 6.7 MHz. But Nosenchuck claims that by air-cooling them to slightly below room



CRUNCHING. Princeton's Nosenchuck (left) and Littman have a 60-gigaflops board and full nodes in the works.

temperature and tightening power-supply margins, he can drive the circuits at 20 MHz to get a peak performance of 480 megaflops per node. Benchmark tests indicate sustained performance of 400 megaflops, he says.

The nodes are connected through the register files in the switch array. Requests for data not available locally are recognized by the switch and sent to a cache buffer. The buffer interrogates neighboring nodes and can have the data ready by the time the original request propagates through the registers in the switch. Even nonlocal data can be accessed like local memory, although node-to-node communication is still constrained by the 500-Mb/s bandwidth of the fiber-optic path that links them.

TURBULENCE. NASA originally funded Nosenchuck and his colleagues to build a high-performance machine that would simulate the transition to turbulence in fluid flows. It soon became apparent, however, that the machine could reach high efficiencies in a wide range of numerical problems—problems that are numerically intensive, amenable to vector processing, and somewhat local in nature so they can be partitioned among many processors.

More than two thirds of the problems now run on supercomputers for simulation, image processing, and graphics are of this type, Nosenchuck says. Commercial supercomputer makers say these problems require the precision of 64-bit floating-point arithmetic, but Nosenchuck contends that the 32-bit precision of the Am29325 is more than enough.

"Our algorithms iterate to converge on an answer, which is the same at 7-digit single-precision or 15-digit double precision," he says. He adds that wrong answers can be guarded against by checking boundary points with double-precision arithmetic.

Algorithms that converge are a luxury, contends Robert Schuhmann, president of Scientific Computer Systems Corp., Wilsonville, Ore., which makes a 64-bit minisupercomputer. "Most applications require 64 bits to get the right answer," Schuhmann says. "It takes a lot of time to write algorithms to make them converge in 32 bits."

Nosenchuck counters that such algorithms frequently use recursive functions, where a result is immediately fed back into the next operation. The AMD chips are uniquely able to run recursive algorithms. The 29325 has a flow-through architecture with two inputs, one output, and no intervening pipelining. "That opens up a whole range of algorithms not even possible for a supercomputer such as a Cray, where results take several clocks," he says. "Even two clock cycles is one too many."

The switch that makes it possible to move data around so quickly is a network with Benes topology—a nonblocking, dynamically reconfigurable net in which any two inputs and any two outputs may be connected simultaneously. For 16 inputs and 16 outputs, a Benes network must have 56 crosspoint switches. In the Princeton machine, they are arranged as an 8-by-7 array of register files, with each file containing 32 registers of 32 bits each.

This net makes it possible for any processor to request any data and get it seven clock cycles later. If the data is in another node, the cache buffer has seven clocks to find it and store it in the seventh row of registers. Once the switch pipeline is full, processing goes on at the rate of one floating-point operation per clock cycle.

The Princeton team—Nosenchuck, associate professor Michael G. Littman, two graduate students, two technicians, and a part-time systems programmer—has been working under the $750,000 NASA contract since July 1984. They have built a three-processor prototype, from which they say they obtain the predicted 60 megaflops, as well as a system of four smaller nodes to test internode communications.

Nosenchuck is considering a commercial venture to build a 128-node system, which would deliver a sustained 50-plus gigaflops and could be built for $50,000 to $75,000 per node, he says. The Princeton group may seek financing to do that after satisfying its NASA contract.

"We want to use these nodes," Nosenchuck says. "A complete system would clearly be the biggest supercomputer in the world." *–Clifford Barney*

FUJITSU TOPS IBM's SIERRA IN PRICE/PERFORMANCE

TOKYO

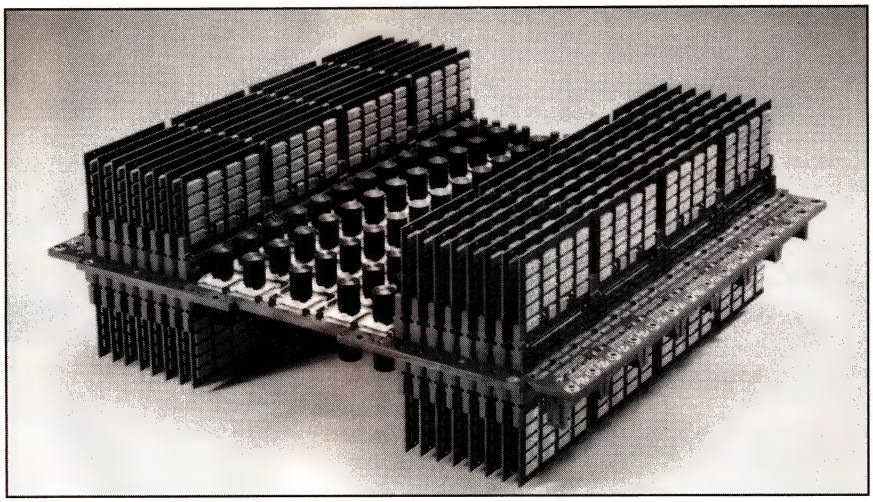
Add Fujitsu Ltd. to the list of computer makers that intend to match mainframes with IBM Corp.'s top-of-the-line 3090 Sierra series. The Tokyo company touts its largest machine as having almost two times the throughput of the most powerful Sierra model, the 3090/400, which hums along at 50 million instructions per second or more.

What's more, Fujitsu maintains that it will price the machines at least 20% below IBM's for equivalent performance. An equivalent Hitachi machine had only a 5% price advantage when it was introduced last spring.

Fujitsu entered the arena in mid-November, announcing shipments of its next-generation IBM-compatible M-780 series by early 1987. Monthly rentals run from $345,000 to $1.2 million.

At the unveiling, Fujitsu had more than just price/performance to talk up. Company officials point out that they have packed the central processing unit on a single liquid-cooled board. Otherwise, the new machine is fully air cooled.

And Fujitsu indicated that it would wean its machines from complete dependence on IBM-compatible software by offering the C language and AT&T Co.'s Unix operating system on its existing and future machines by the end of 1986. Enhancements to Cobol compilers are also being offered, however, indicating that the weaning will not be abrupt. Also heavily emphasized were Fujitsu's communications capabilities, including new packet-switching hardware conforming to the open-systems interconnection reference model (OSI).



KEEPS COOL. An air-cooled memory module for Fujitsu's M-780 mainframe carries 55-ns CMOS 256-K static RAM with n-MOS arrays. Their speed eliminates the need for a cache.

THE BUS ARCHITECTURE CAREER COMPATIBILITY TEST.

At the low end of Fujitsu's new series comes the M-780/10s, a single processor that the company claims is equivalent in processing power to IBM's dyadic entry-level 3090/200, which is rated at more than 30 mips. Two of the entry-level machines working as a dual processor are equivalent to the upgraded 3090/400.

But that is only the beginning of the story. A higher-performance M-780/10 with 1.3 times the power of the M-780/10s will be available with one to four processors. Field upgrades are available from the smallest M-780/10s to the largest M-780/40. Surprisingly, Fujitsu will not say whether it will offer an integrated array processor for vector processing with the new system.

This performance should put Fujitsu ahead of or even with its domestic competitors. Hitachi Ltd., for example, claims performance at least equal to the IBM 3090/400 for its dual-processor M-682H [*ElectronicsWeek*, March 18, 1985, p. 16]. Hitachi has not announced a four-processor version, but industry sources say that Hitachi probably would do so

Efficient IC packaging helps hike the speed of Fujitsu's machines

should an important customer want one. Specifications for the M-780/40 put it about even with the largest system in NEC Corp's ACOS 1500 family, which also has a claimed performance of twice the 3090/400 [*ElectronicsWeek*, March 11, 1985, p. 16].

CHIPS ARE KEY. Efficiently packaged high-performance chips are central to the system's speed. The entire CPU is fabricated with up to 336 integrated circuits on both sides of a 540-by-490-mm printed-circuit board with 42 wiring layers. Still, Fujitsu engineers say they can cut traces and add jumpers for upgrades, as Hitachi can do on its dense supercomputer boards [*Electronics*, Nov. 11, 1985, p. 26].

Logic chips that dissipate 9.5 W have either 3,000 or 10,000 gates with a propagation delay of only 180 ps per gate. Cache-memory chips provide 16-K of random-access memory with an access time of only 3.2 ns and 1,200 logic gates on the same chip.

Main memory, for the first time in a general-purpose computer, uses high-speed static-RAM chips. The 256-K SRAMs have an access time of only 55 ns, eliminating the need for the global cache used in Fujitsu's previous-generation M-380 mainframes.

Chip packages on the CPU board measure 22.5 by 22.5 mm and have 180 leads with centers spaced only 0.4 mm apart. This is an even finer pitch than the 20-mil (0.508 mm) lead pitch of the high-density packages in Hitachi's M-680 computers.

In a break with previous practice, Fujitsu sandwiches the CPU between two conductive cooling modules that make contact directly to each chip package. Liquid coolant carries the heat to a coolant distribution and control unit, where it is typically released to the air.

Fujitsu engineers stress that the computer can be air cooled because it dissipates less total power than previous systems. Liquid cooling is required within the system only where heat is concentrated because of high packing density. Other boards have a lower packing density and use multiple-fin packages where required to transfer heat directly to the cooling air stream. *–Charles L. Cohen*

SEMICONDUCTORS

IBM FIRES HOT ELECTRONS THROUGH COOLED GaAs

YORKTOWN HEIGHTS, N. Y.

The operating speeds of semiconductors could increase fivefold with the ballistic electron-transfer techniques under development at IBM Corp.'s Thomas J. Watson Research Center.

IBM researchers have demonstrated physically what solid-state theoreticians have been saying for years: that given a thin enough layer of semiconductor material, electrons can be shot through it without encountering any resistance whatsoever [*ElectronicsWeek*, April 1, 1985, p. 22]. Because a large proportion of the traveling electrons avoid vibrations and collisions with impurities in the semiconductor medium, their speed isn't compromised.

With current technologies, electrons typically scatter as they travel through the semiconductor, losing amplitude and direction. But Mordehai Heiblum, an IBM research staff member who has spent the last seven years studying ballistic electron transfer, found that when he injects "hot," or excited, electrons through thin, cooled layers of aluminum gallium arsenide and GaAs sandwiched into a device 0.13 μm thick, more than 40% make it through without measurable energy loss.

LAYERED STRUCTURE. "Naturally, we would like to get it to 100%, but 40% to 50% is good," says the Israeli-born Heiblum. He chose the vertically layered structure—which resembles that of bipolar devices—because it is more accommodating to electron-beam injection techniques.

The experiment begins with cooling the "hot-electron device," as IBM calls it, to 77 K in a liquid-nitrogen bath. That retards the movement of the individual atoms within the structure, which in turn reduces resistance. "The movement of the atoms and lattice movement are quieted down as compared to ambient temperatures," says Heiblum.

He injects the cooled device at varying voltages by way of gold-germanium contacts. The injected charge travels through a 0.03-μm-thick layer of GaAs and into a 0.1-μm-thick layer of AlGaAs in about 0.03 ps, a rate equal to about

LIKES THEM HOT. IBM's Heiblum injects excited or "hot" electrons into an experimental device to see how many come through a thin GaAs layer at undiminished (ballistic) speeds.

DO YOU ENJOY SPENDING NIGHTS AND WEEKENDS ALONE CONFIGURING YOUR SYSTEM?

Career Compatibility Test			
Bus Capability	*VME**	*MB II*	*Mark Your Preference*
Geographic Addressing		*X*	
Built-in Self-Test		*X*	
Software Configurability		*X*	

Do you enjoy hunting down a misplaced or missing jumper at 2 o'clock Saturday morning?

If so, don't choose the MULTIBUS® II architecture.

Because the MULTIBUS II architecture has an exclusive feature that reduces or eliminates jumpers and dip switches.

It's called geographic addressing. And it allows boards to be addressed by slot number in software, which eliminates or greatly reduces jumpers. For example, there are no jumpers on the entire line of MULTIBUS II memory boards.

But if you do need jumpers, geographic addressing can still help. Because software can use it to verify correct jumper placement.

And not only is board configuration fully supported in software, but so is identification of board type, manufacturer and the revision level of both hardware and firmware. Geographic addressing also provides a capability for built-in self-test and remote system diagnostics.

Making things a lot easier for you. And resulting in lower test costs and improved serviceability.

But, by all means, if you enjoy tearing your hair out while re-reading the manual for the umpteenth time, catch the other bus.

It doesn't have geographic addressing, so you could find yourself knee deep in jumper and testing problems. Which means you'll spend many long, gratifying nights working at your bench.

Now, indicate your bus choice in the preference box and turn the page.

*Source: IEEE P1014 Draft 1.2, August 1985.

© 1985 Intel Corp.

10^8 cm/s, or five times the speed of electrons in current transistors, says Charles Kircher, manager of exploratory III-V devices, who is responsible for overseeing Heiblum's research.

The layer of AlGaAs underneath the superthin layer of GaAs poses a physical barrier that can be increased by applying a direct external voltage to the second layer. Heiblum adjusts that voltage to the point at which the barrier layer stops all electrons whose energy levels are below the levels at which they were injected originally. He can then calculate the percentage of those electrons that were able to surmount the barrier—meaning they encountered no resistance—from his measurement of the current at the output point.

The device, which operates at low temperatures only and not at ambient temperatures, has no load or capacitors. It is designed with a simplified architecture to enhance its value as an experimental tool, says Heiblum.

There is still a long road for Heiblum and his associates to travel before ballistic devices emerge from the laboratory. "I don't think we know enough at this point to talk about time scale," admits Kircher. But the work so far dovetails with Kircher's belief that the high-performance computers of the future will run at similarly low temperatures.

Kircher says the thicknesses of the different layers are exaggerated in the experimental device, but he maintains that layers of GaAs 0.5 μm thick could work for a ballistic transistor and that silicon could be used if thicknesses were kept below 0.1 μm.

For his part, Heiblum has a more futuristic bent, calling the device, which is constructed using molecular-beam epitaxy in a clean room not far from his laboratory, an "electron spectrometer." He explains that at this point it is purely a research tool. "The device's structure is one we can use to see how we can apply [this technology] in other ways." *–Tobias Naegele*

EXPERT SYSTEMS

MDs' AI TOOLS STILL NEED DOCTORING

BALTIMORE

The medical office of the future is likely to boast expert systems that help doctors diagnose illnesses, and researchers are now testing more than a dozen prototypes of such systems in clinical settings. Yet they admit it will take still further evaluation to determine whether these diagnostic systems improve patient care.

"The evaluation of [these] systems is an open research area, and will remain so for the foreseeable future," said Perry L. Miller of the Yale University School of Medicine.

Miller chaired a panel on AI systems in medicine during a mid-November symposium held in Baltimore on computer applications in medical care. Panelists reported high levels of agreement between expert systems and specialists in fields ranging from neurology to rheumatology. Although panelists stressed that evaluation criteria are only now being developed for each system, they also said they are learning lessons that can be applied to future systems.

"There are general principles emerging from this work that are applicable in other areas" of medicine, said Edward H. Shortliffe of the Stanford University Medical School. Since 1979, Shortliffe and an interdisciplinary research team have been developing a cancer chemotherapy planning program called Oncocin at Stanford's Oncology Clinic. The program is designed for clinical use with cancer patients who are receiving experimental treatments under a research protocol.

A redesigned version for single-user Lisp machines will replace the prototype later this year and include what Shortliffe calls a "temporal network." The network is to provide the system with a method for obtaining vital data about a patient's past—such as repeating cycles of chemotherapy or sequential radiation therapy. "This program must be able to reason about the patient's past treatment history in order to generate a therapy plan that is responsive to the problems he or she may have encountered in the past."

Shortliffe and other researchers said some factors that need to be demonstrated in evaluating medical consultation systems are:

- A need for the system.
- System performance at the level of an expert, the so-called "gold standard."
- The system's usability.
- Acceptance of expert systems by physicians.
- The system's impact on the well-being of patients.
- Cost-effectiveness.

Computer diagnoses aren't yet as good as human experts'

"It's pretty hard to show that a system is usable if it's not operating at the level of experts," said Shortliffe. Yet a gold standard for expert systems is difficult to attain because clinicians and specialists seldom come to universal agreement. Just as useful would be a set of benchmark cases within a knowledge base that contains classic examples of each disease, said Lawrence C. Kingsland of the National Library of Medicine's AI/Expert Systems Program.

Kingsland described the evaluation of a consultant system in rheumatology called AI/Rheum. The system's structured knowledge base contains formal criteria for 26 rheumatologic diseases. Kingsland reported that the agreement of the AI/Rheum system with the gold-standard diagnosis of clinicians exceeded 90% during three sets of clinical cases. The system is now being transferred from a DECsystem 2060 mainframe at Rutgers University, where early development took place, to Digital Equipment Corp. VAX-11/780s at the National Library of Medicine in Bethesda, Md., where validation of the knowledge base will continue.

For the last year and a half, University of Maryland Hospital researchers have been evaluating another expert system used to identify transient ischemic attacks (TIAs), brief malfunctions of the nervous system that often lead to strokes. James A. Reggia of the hospital's Department of Neurology said their evaluation of the system, which diagnosed 100 patients who suffered TIAs, measured agreement with neurology specialists, not the accuracy of the diagnosis. Reggia prefers statistical measurement of agreement over accuracy because specialists often disagree, making it "very difficult to define a correct answer."

DISCREPANCIES. Although the system registered "excellent agreement" (86%) with the diagnoses of stroke specialists, discrepancies arose in treatment recommendations. Nevertheless, Reggia contended that even the discrepancies suggest that expert systems have the potential "to influence patient care by providing a second opinion." He added that it would be relatively simple to incorporate alternate decision-making criteria into the TIA system to provide users with multiple opinions on the same patient.

Other medical expert systems making the rounds include Mycin, used to diagnose and recommend treatment for infectious diseases; Caduceus, formerly the Internist, one of the earliest medical systems used in internal medicine; and AI/Gen, used by geneticists to diagnose

DO YOU LIKE THE CHALLENGE OF RELIABILITY PROBLEMS?

Career Compatibility Test			
Bus Capability	*VME**	*MB II*	*Mark Your Preference*
Power and Ground Pins (PI Connector)	*14*	*30*	
Synchronous Protocol		*X*	
Bus Parity		*X*	

Somebody switches on a compressor and your computer system dies.

Swell. Is that the kind of career challenge you got into the systems design business for?

If so, don't choose the MULTIBUS® II architecture. Because MULTIBUS II systems ensure reliability in three ways.

First, a large number of power and ground pins provides superior signal quality.

Then synchronous protocol gives you increased noise immunity. And protects you from metastability problems.

Finally, bus parity protects against disturbances on any line. Whether it's address, data or control.

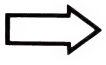
On the other hand, if dealing with reliability problems gets your blood pumping, the other bus should give you plenty of satisfying excitement.

It has only 14 power and ground pins compared to 30 on the MULTIBUS II boards. And it doesn't offer you the protection of synchronous operation or bus parity. Which means metastability becomes something to watch out for. The other bus can be very challenging indeed.

Indicate your preference and continue.

*Source: IEEE P1014 Draft 1.2, August 1985.

© 1985 Intel Corp.



hearing- and sight-loss diseases.

Now that clinical evaluations are under way, researchers are also looking to foster wider acceptance of medical expert systems among physicians. One inducement, said Kingsland of the National Library of Medicine, would be their time-saving integration with patient data bases contained in hospital information systems. "That level of integration," he stressed, will be needed for widespread acceptance.–*George Leopold*

PERIPHERALS

KODAK RAISES ITS STAKE IN THE SMALL-DRIVE GAME

ROCHESTER, N. Y.

Eastman Kodak Co. is making a big play in the mass-storage market with three high-density floppy-disk drives. The photography giant has a foothold in floppies, but the new family marks a major commitment in the volatile disk-drive market.

Kodak's strategy is to fill a niche by combining innovations in electronics, mechanics, and media technology to obtain reliable multimegabyte storage from floppy disks, explains Peter Giles, vice president and general manager of Kodak's Mass Memory Division.

The most impressive of the three Kodak drives is a unit that stores 12 megabytes (10 formatted) on a 5¼-in. removable floppy disk, which will make inroads into territory held by hard-disk drives. The Kodak drive, model 12.0, is reminiscent of the Bernoulli Box drives made by Iomega Corp., Roy, Utah, although Iomega extracts 20 megabytes from a 5¼-in. floppy disk. Both Kodak and Iomega protect the floppy disk with a hard plastic case; both use embedded servo-positioning techniques to boost track density; and both use voice-coil head-actuator technology to cut access times.

Kodak's drives do not, however, maintain a cushion of air between the head and the disk surface, as do Iomega's drives. And they spin the disk at 600 rpm, compared with 1,800 rpm for Iomega's.

Like Iomega's products, Kodak's new 12-megabyte model competes with low-end Winchester drives in terms of both capacity and speed. It sports an average access time of 75 ms and transfers data (internally) at 2 Mb/s. It will be available by the end of next summer, says a Kodak spokesman.

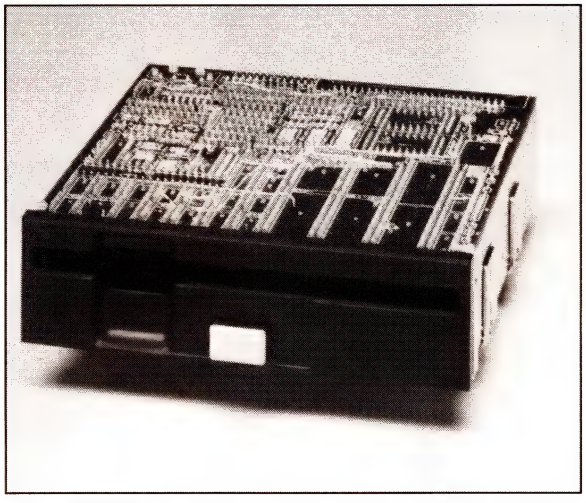
One innovation that helps the model 12.0 to store 10 megabytes is a patent-pending variable-rate recording process. The drive increases the recording speed for the outer tracks and slows it down for the shorter inner tracks.

The 12.0 drive, which has a built-in controller with a Small Computer System Interface, was developed in conjunction with Data Technology Corp. of Santa Clara, Calif., in a cooperative venture funded by Kodak. "Our joint contribution will benefit users who have been seeking a viable alternative to hard drives and low-storage-capacity floppy drives," says David Lee, the new chief executive officer of Data Technology.

All three Kodak drives use a high-coercivity (600 Oe) disk medium developed by Verbatim Corp., Sunnyvale, Calif., which was acquired by Kodak last June. For the 12.0 drive, the disk has two write-protect zones that allow the user to safely store applications programs on one part of the disk and data on the other.

Verbatim preformats the disks with a code that marks either side of a track with a code at the start of each sector. The code is used by the drives' proprietary track-following servo system.

TWO STEPPERS. The less-capacious members of the drive family store 3.3 and 6.6 megabytes, or 2.78 and 5.24 megabytes formatted. Both use novel head positioners with two stepper motors each—one for coarse positioning and the other for fine positioning. The 3.3-megabyte unit is available now for $285, and the 6.6-megabyte version will be available in the second quarter of 1986.



IN THE PICTURE. Kodak aims for a share of the small-drive market. The model 12.0 puts 10 megabytes on a floppy disk.

The fine-adjustment stepper motor can move the head assembly in increments as small as 200 μin. The 3.3 and 6.6 drives have track densities of 192 and 384 tracks/in., respectively. Both the 6.6 and the 3.3 offer downward read compatibility, which allows users to read data stored on drive-and-media combinations such as those used in IBM Corp.'s Personal Computer and PC AT.

In Kodak's view, the new drives' speed and capacity will allow the company to succeed in a market known as less than kind to new entries [*Electronics*, Nov. 18, 1985, p. 85]. "We feel Kodak drives fill an important gap caused by the low capacity of traditional floppy drives and the lack of removability of hard drives," says Giles. "Our systems provide effective and efficient primary, backup, and add-on solutions for data-storage problems." –*David M. Weber*

COMPONENTS

CUTTING THE COST OF TOUCH PANELS

GLENVIEW, ILL.

Touch screens have been around since the mid-1970s as an alternative to keyboards for interacting with computers. Yet despite products with touch-screen capability from the likes of AT&T, Digital Equipment, and Hewlett-Packard, the technology so far has not taken off in a big way, largely because of relatively high prices. Now several vendors are vying to breach that barrier.

Zenith, Tektronix, and the ITW Entrex division of Illinois Tool Works Inc., Chicago, all showed products at last week's Wescon show in San Francisco that are geared toward driving down the cost of touch technology. Tektronix Inc.'s product improves on existing membrane-based technology, while the Entrex screen is based on a modified optical-sensing technique. Zenith Electronics Corp., however, is going with a whole new technology based on surface acoustic waves.

Zenith will offer what it calls an "acoustic touch system" to original-equipment manufacturers for just $150 in 2,000-unit quantities—half the price or less of most systems. What's more, by exploiting SAW properties, the Zenith panel will add an extra dimension to touch technology because the screen responds to the amount of pressure applied. Indeed, Zenith bills the panel as the industry's "first truly three-dimensional touch system."

To date, no other vendors offer touch

DO YOU CHERISH MULTIPROCESSING LIMITATIONS?

Career Compatibility Test			
Bus Capability	*VME**	*MB II*	*Mark Your Preference*
Virtual Interrupts		*X*	
Number of Interrupt Levels	*7*	*255*	
Distributed Arbitration		*X*	
Number of Arbitration Levels	*4*	*20*	

Does the anguish of running out of interrupts give you a masochistic sense of pleasure?

If so, stay away from the MULTIBUS® II architecture.

Because of its virtual interrupt feature, MULTIBUS II boards give you all the sources and destinations of interrupt you need for multiprocessing. Up to 255.

And to make it an even stronger candidate for multiprocessing, the MULTIBUS II architecture features distributed arbitration. Which assures that no single board can hog the bus. In fact, MULTIBUS II systems are so flexible they can easily accommodate up to 20 bus masters.

Of course, if you believe that needless frustration builds character, you should choose the other bus.

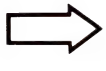
You'll be stuck with a dedicated interrupt arrangement that effectively allows you only seven interrupts. And because it uses central arbitration, you're effectively limited to only four masters.

Of course, if you want to design systems that are more powerful, useful and flexible, you should choose the MULTIBUS II architecture.

Now turn to the last page and complete the test.

*Source: IEEE P1014 Draft 1.2, August 1985.

© 1985 Intel Corp.



products matching Zenith's three-axis system. But both Entrex and Tektronix, among others, hope to drive prices down on conventional X-Y-axis touch systems, which use membrane or optical techniques and typically sell to OEMs for $300 to $500.

Tektronix entered the touch-panel business with a membrane-based product called TekTouch that uses a method for depositing a continuous resistive film made of proprietary material directly onto a cathode-ray-tube screen [*Electronics,* Nov. 18, 1985, p. 98]. The company promises to sell the system in volume for significantly less than $300.

Entrex used Wescon to promote its Cyclops touch-panel system, which went on the market in small production quantities last July. By using far fewer components than conventional optical-sensing systems, Cyclops costs less to produce, says Entrex. A 13-in. diagonal version is now being offered at about $120 each in 2,000-unit quantities.

THE Z FACTOR. Zenith's system also costs less than conventional optical and membrane-based systems. But the use of SAWs throws in a bonus—the Z coordinate. This means it can also detect the amount of finger pressure being applied. For example, an office user could scroll text slowly by pushing gently on the screen or scroll quickly by applying more pressure; similarly, an engineer might zoom in to progressively greater detail on a drawing.

Surface acoustic waves let Zenith touch panel detect finger pressure

The Z-coordinate capability comes from the natural plasticity of the human finger and the fact that it absorbs energy when it interrupts a SAW, says James J. Fitzgibbon, a project engineer at Zenith's Systems & Components Group. The system relies on two corner-mounted piezoelectric elements that are electrically excited to emit 4-MHz SAWs in 4-ms bursts.

The waves travel across the screen surface and bounce off acoustic-reflector strips around the tube periphery. What comes back to two piezoelectric detectors mounted in the tube's other two corners is an extended wave of about 150 μs that is a time expansion of the SAW bursts originally sent out, says Fitzgibbon.

When a finger touches the screen it absorbs energy, creating a "dip" in the return wave. The system's microprocessor times the dip to calculate the location of the touch. The finger spreads out as it presses harder, covering more screen area and absorbing more energy.

Zenith says the SAW touch system can be customized for installation on 5 to 25-in.-diagonal displays. It will be offered with up to 50 touch points/in.^{2} and up to 16 pressure levels per screen.

With its move into the touch-panel business, Zenith is entering a slow-moving market. Industry sources say about a dozen U. S. companies will compete for only about $15 million in sales this year. That figure could climb to $100 million in the next five years or so, say market watchers.

With its $150 price point and by offering Z-coordinate capability, Zenith hopes its system will drive the market. The company sees uses for its acoustic touch panel in traditional applications such as public information systems and automatic teller machines, but also increasingly for jobs in personal computers, dashboard-mounted displays, computer-aided-design terminals, and industrial-control systems. *–Wesley R. Iversen*

GRAPHICS

TARDY UK BOARD MAKERS DRAW A BEAD ON OEMs

LONDON

European companies so far have made little headway in the market for high-performance graphics work stations, and it might be too late for them to succeed now. So rather than take on larger, established competitors directly, two British startups are trying to enter the burgeoning computer-graphics business through the back door. Both Benchmark Technologies Ltd. and Primagraphics Ltd. are selling high-performance computer-graphics engines for incorporation into gear made by other original-equipment manufacturers.

Benchmark, of Kingston upon Thames, Surrey, launched its first product, a graphics engine capable of 80 million instructions per second, at the Compec '85 computer show held in London earlier this month. Primagraphics, of Royston, Hertfordshire, recently scored its first OEM success with a significant contract from Racal Norsk Ltd., the Anglo-Norwegian computer maker, and at the time of Compec was close to signing another OEM contract with a UK work-station manufacturer.

The computer-graphics market is growing and segmenting rapidly, with products ranging across the spectrum in both price and performance. The British game plan has focused on the market for high-resolution graphics—1,000 by 1,000 pixels and more—achieving high performance with multiple bit-slice microprocessors. Such resolution and performance are needed in image processing, the printing industry, and command and control applications such as air-traffic control, video graphics, animation, and high-performance work stations.

Primagraphics is also seeking, on its own account, other outlets for its Topaz graphics engine. Linked with a video camera, for example, Topaz can digitize and store maps, engineering drawings, and the like. The camera is mechanically scanned across documents by a precision lead screw. The documents can then be archived on video or digital media and easily updated. "Utilities can overlay pipelines and civil works on survey maps. Also, hospitals are interested in the technology for storing X-ray images," says Roy White, Primagraphics' managing director.

Primagraphics has also developed a video-frame grabber that digitizes TV-standard images at the full frame rate. When the frame grabber is hooked to a Topaz system, the setup can be used for TV graphics and animation.

DESIGNERS. Benchmark Technologies was formed in 1984 to design minicomputer systems on an OEM basis for other manufacturers. The founders' idea was to farm out both manufacturing and marketing, leaving the company free to concentrate on design.

Benchmark has designed a single-board engine using AT&T Co.'s Unix operating system as well as its single-board image-processing engine. The Unix engine can be used as a controller for the graphics processor to form a self-contained system. Or the graphics processor can be hung off a standard bus such as the Q-bus or that of

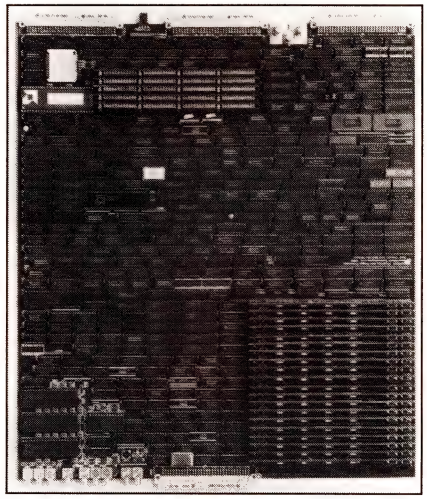


IMAGE POWER. Up to eight 10-mips Benchmark graphics boards can work together.

DO YOU THINK GUARANTEED COMPATIBILITY IS FOR SISSIES?

Career Compatibility Test			
Bus Capability	*VME**	*MB II*	*Mark Your Preference*
Synchronous Protocol		*X*	
Spec Options	*Many*	*Few*	

When a board from manufacturer X doesn't work with a board from manufacturer Y, do you secretly get a perverse sense of delight?

If so, you won't be happy with the MULTIBUS® II architecture.

Since it has a synchronous protocol. Which not only provides noise immunity, but compatibility as well.

In fact, synchronous protocol, because of the very rigorous definition it requires in specs, virtually guarantees compatibility among MULTIBUS II boards from different vendors. And across many generations of VLSI. Assuring a long life for your products.

The other bus has a very unconstrained asynchronous protocol. With lots of spec options. Which gives board manufacturers lots of "leeway." So all sorts of delightfully unpredictable things can happen. For instance, bus timing can change when boards are added or removed from the backplane. Signal edge rates can change too. And options can lead to incompatibilities.

Of course, maybe you think putting up with that kind of frustration is what you trade for higher performance.

Not so. The MULTIBUS II architecture can run faster than the other bus.

So mark your preference now. We'll wait. Then put your pencil down because this is the end of the test.

If you chose the MULTIBUS II architecture more often, read on. If you chose the other bus more often, you might consider a new career direction (or a good course in stress management).

Still with us? Good. Want to learn more? Then call or write for our MULTIBUS II Technical Series: Intel Corporation, Lit. Dept. W262, 3065 Bowers Ave., Santa Clara, CA 95051.

Or call toll-free now at (800) 538-1876.

It's the best career move you can make.

intel®

*Source: IEEE P1014 Draft 1.2, August 1985.

© 1985 Intel Corp.

the IBM Corp. Personal Computer AT.

The company offers its Unix board with a choice of 32-bit processors—National Semiconductor's 32032 or 32332, Motorola's 68020, or Intel's 386. All run Unix System V.2 at 16 MHz. A secondary 80186 processor on the card runs MS-DOS 3.1 concurrently.

Benchmark has packed its Graphics Image Processor (GIP) onto one board by employing the latest video chips, such as dual-ported random-access memories and color look-up chips. The heart of the subsystem is a 29116 bit-slice processor capable of about 10 mips. It uses a writable control store, so the user can optimize the microprogram; Benchmark provides an assembler for this purpose.

The GIP, which sells for about $7,000 in single units, supports a 1,280-by-1,024-pixel 60-Hz (noninterlaced) screen. It carries eight bit planes, so up to 256 colors can be displayed at once. Its block-fill rate is 20 billion pixels/s.

Up to eight GIP boards can be cascaded to achieve a total image-processing capability of 80 mips. Conversely, a single board can be shared by eight monochrome terminals, each having sole access to one bit plane. This approach could be used where high resolution at modest cost is needed. The GIP's performance flexibility has already attracted the interest of U. S. equipment suppliers.

Primagraphics' Topaz system also uses bit-slice processors with a writable control store, but it is assembled from six VMEbus board types. It can be controlled by its own 68000-based card or other processors on the VMEbus.

As does Benchmark, Primagraphics uses a hierarchic bus structure to avoid communications bottlenecks. Control is exerted through the VMEbus, while image data is carried on another bus running at 15 megabytes/s. The company is now getting a memory board ready that combines color look-up functions with 4 megabytes of memory on a single board, which takes three cards with the present line. *–Kevin Smith*

MICROCONTROLLERS

MADE-TO-ORDER CONTROL ICs MOVE IN

AGRATE, ITALY

Italy's principal semiconductor-components manufacturer is about to play a card that could change the nature of the market for microcontrollers. In the final design stages at SGS Microelettronica SpA is a family of one-chip microcontrollers that customers can configure to suit their applications.

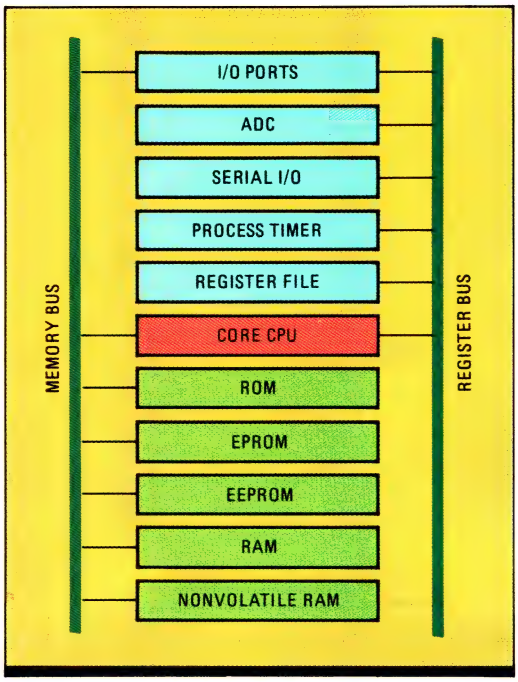
Thanks to the chips' dual-bus structure and SGS's library of peripheral functions, customers have wide latitude in structuring their chips. Because the result approaches a dedicated circuit, performance is maximized. Because the customer pays only for the functions he chooses, his costs drop substantially.

DRASTIC CUTS. For low-end applications in which only a minimum of functions is necessary, this means that the microcontroller could cost as little as $3 per circuit, says Giancarlo Forlanini, the company's MOS division microprocessor-product marketing manager. For applications using the entire SGS library of functions, the figure rises to about $25, though he says the cost would be at least $40 for a comparable level of functionality using standard microcontrollers and associated peripherals.

SGS's reason for developing a new microcontroller in a market that hardly looks underpopulated derived from the observation that existing microcontrollers are based on the cores of standard microprocessors and are thus burdened with certain limitations. One limitation, says SGS's microprocessor-design manager Paolo Rosini, is their notorious resistance to on-chip expansion because they were designed originally as an integral part of a family of circuits. Another, he says, is that few of them can operate efficiently using external memory because they have to devote a large number of input/output lines to a connection with the external memory.

The SGS microcontroller family—the most powerful of which carries the designation S9—was designed for maximum flexibility. Each chip will carry the system CPU, a memory bus where commands are accessed, and a register bus where they are executed. The CPU's internal architecture uses a combination of 8- and 16-bit data paths and communicates with the outside world by way of an 8-bit bus. A 24-MHz external oscillator drives its 12-MHz internal clock. Instruction-execution time is an impressive 0.83 μs.

The user can then choose the combination of read-only memory, erasable programmable ROM, electrically erasable PROM, static random-access memory, and nonvolatile RAM he requires as on-chip memory up to a maximum of 16-K bytes. To the register bus he can connect the appropriate combination of register files, timing controllers, serial I/O communications controllers, parallel I/O ports, and analog-to-digital converters. In addition, SGS plans to offer a library of dedicated peripherals.



BETWEEN THE BUSES. SGS's S9 microcontroller consists of independent modules connected by two buses.

MULTIPLE APPLICATIONS. Mario Licciardello, MOS division product manager for microprocessors and logic devices, expects the S9 family to find low-end applications in the consumer field, and medium- to high-end applications in telecommunications, automation and robotics, and digital TV. The only areas he believes it will not be worth considering are standard microprocessor applications for which there is already a large body of software, such as data-processing systems based on established operating systems such as MS-DOS.

SGS executives know they face a tough task in garnering acceptance for a new family of microcontrollers, particularly from equipment manufacturers who have long been using another family. To help ease the way for the S9 family, SGS will also offer a low-cost development tool that can turn any IBM Corp. Personal Computer, Digital Equipment Corp. VAX, or Unix-based computer into a development system. Because the development software features a C compiler, software for the S9 family will be relatively easy to code for any programmer accustomed to working in that language.

The S9 family will be fabricated in 1.5-μm n-well CMOS. SGS expects to offer samples around the third quarter of 1986. *–Robert T. Gallagher*

LOOK WHO'S BACK.

ELECTRONICS IS BACK.

WITH THE INDUSTRY'S LEADING COVERAGE OF INTERNATIONAL TECHNOLOGY.

During the first half of 1985, Electronics—with its worldwide bureau of correspondents—published more than 140 articles on international technology, including:

January

Philips Uses MBE for Lasers

Siemens Readies Commercial ISDN

Japanese Chemical Firm Moves from Soap to Floppies

Italian firm Seeks Allies to Crack U.S.

Japan Persues Role in Space

Bellman Switches on Italtel for Expansion

Robots get Smart in Japan

ITT Invests in European Units Crack US..

February

Europe's Esprit Finally Sets Sail

LSI Logic Counts on Sandfort to make its Mark in Europe

Upstart Vendor Makes Waves in Japan's Robot Market

NEC Fashions New Fab Process

Olivetti's Viti Directs ET Designs that Marry Bus & Art

German Startup's Success Surprises Europeans

Britons Seek Tolerant Chips

OBI Rains on IBM's Parade

Mega's Friedrich Aims to Cut Asian Lead in Memories

March

British GaAs Chips Go to Market

NEC's CPU Leapfrogs IBM

Hitachi CPU Challenges IBM

Yoshida Seeks Yankee Ingenuity for Joint Ventures with Tokyo

Plessey Custom Chips will Test Themselves

France's Lansat Rival Set for Fall Launch

Olivetti Stakes Claim in Video Typewriters

Italian VLSI Chip has the Right Accent

Koreans Try for VCR Replay

Germans Push X-ray Exposure

There's Life in Resistors, German Company Finds

East Germany's Herzog Competes with West for World Markets

UK Beats a Path for Europes Race

April

German System Meets New ICAO Standard

West Germans Squabble Over Choice of IFF

Britain Promotes Open Architecture

US Makes Progress in Japan Telecom Talks

Japan's Lead in Optical Disks: It's Part of the System

Daisenberger Guides US Firms through Red Tape

Asia: It's No Longer Just Japan That Threatens US Markets

Malaysia: Top Shipper of Discretes

Indonesia: Domestic Sales are the Lure

May

Thomson's VCR System Clears Up Doubts

ICL Banks on Networks and Japanese Chips

Philips Gives Boosts to Performance of Multimode Fiber

Min Blazes Bright Path for Korea's Gold Star

Asia: The Four Dragons Rush to Play Catch-up Game

Singapore Casts Lot with Software

Philip's Eurom Chip Finally Debuts

Mitsubishi Etches a Path Toward 4-Mb DRAMs

Sagging Prices Sting Japanese Producers

British Telecom Spreads Its Wings with Mitel

South Korean IC Maker Seeks World Markets

June

Hitachi Set to Ramp Up 64-K Bipolar-CMOS Chip

Plessey Switches Off Flash ADC, Saves Power

Sony Campaigns Hard for BMM Camcorders

Japanese Quit on IBM Software, Turn to UNIX

Apple Tries Again to Blast Off in Japan

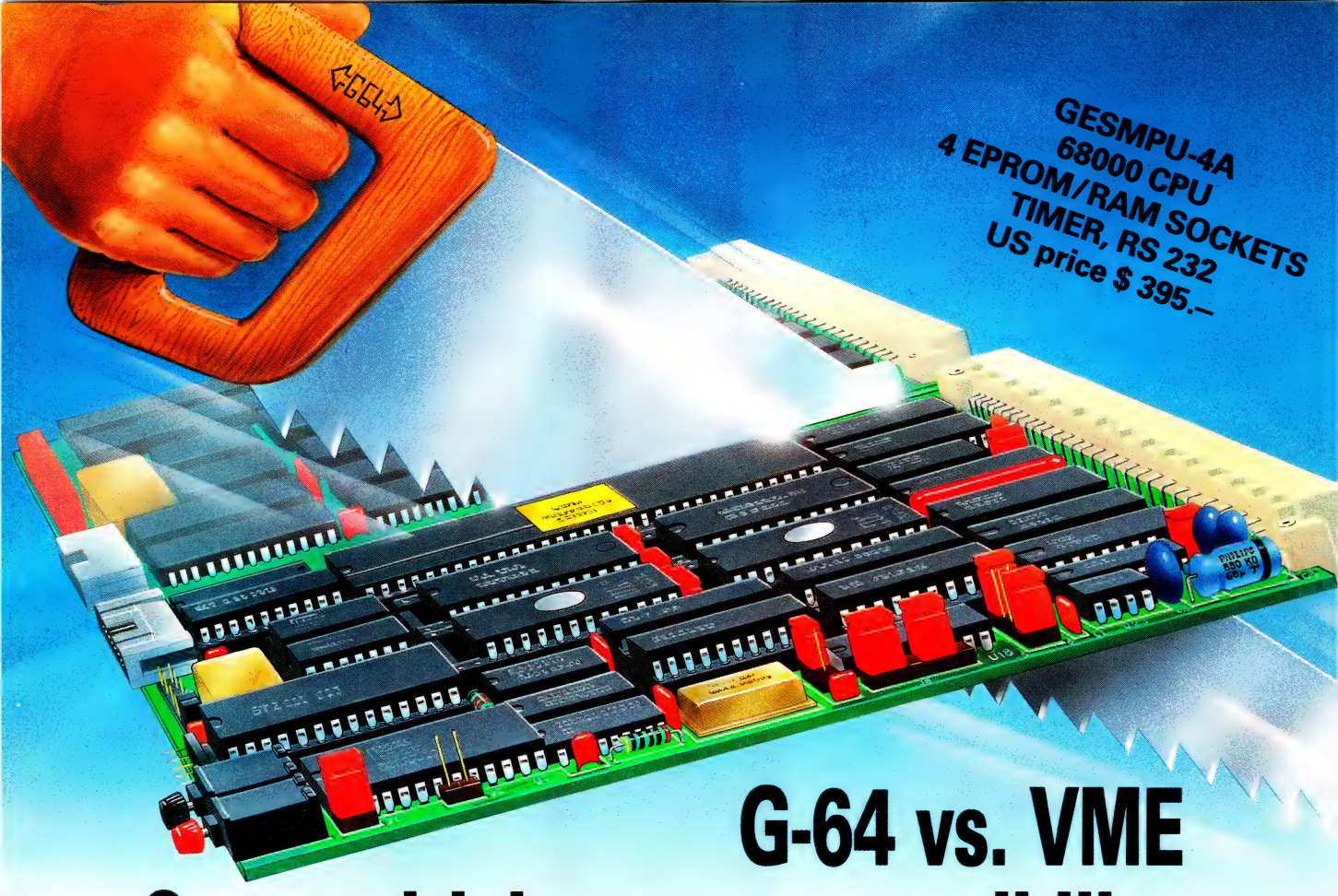
Has the End Come for European Chip Makers?

Jacoel, Picked by Workers, Turns Company Around

SIA Protest May Not Stem Trade Tide

Now It's Korea's Turn in the Robot Market

SHOULDN'T YOU BE BACK?



G-64 vs. VME
Competitivity vs. compatibility

IF VME WAS SMALL, EASY-TO-USE AND INEXPENSIVE, IT WOULD BE THE G-64 BUS

If you are looking for an easy-to-use, processor independent, 8/16-bit bus for your control applications, we agree that VME bus is not the right choice for you. Instead, GESPAC, a pioneer and world leader in Eurocard technology, offers you a competitive alternative: the European standard G-64 bus.

Like VME, the G-64 bus is an industry standard using the same rugged Eurocard form factor and DIN connector. Unlike VME, the G-64 bus is exclusively specified for single height Eurocard for 100x160 mm. Because of the bus' simpler architecture, the smaller G-64 boards offer similar level of performance and functionality than that typically found in VME.

VME IS NO LONGER YOUR ONLY CHOICE

The G-64 bus is the backbone for GESPAC's product line of almost 100 truly different and complementary functions, market-proven and guaranteed to work together. In addition, the availability of **all** the most popular 8 and 16/32-bit microprocessors provide system integrators with the flexibility and the convenience of a one stop shopping unmatched by any other bus.

CUT YOUR COST WITH THE G-64 BUS

Best of all, because the G-64 bus is simpler and easier to use than VME, a G-64 system is typically less than half the cost of an equivalent VME system. An increasing number of OEM's are discovering this every day and many are beginning to use it. Some of them may be your competitors, and with the G-64 bus they are given an unfair advantage to beat you in the market.

DISCOVER GESPAC BEFORE YOUR COMPETITION DOES

Gespac

IN USA – CANADA
100 West Hoover Ave
Mesa, AZ 85202
Tel. (602) 962-5559
Telex 386575

INTERNATIONAL
3,chemin des Aulx
CH-1228 Geneva
Tél. (022) 713400
Telex 429989

INSIDE TECHNOLOGY

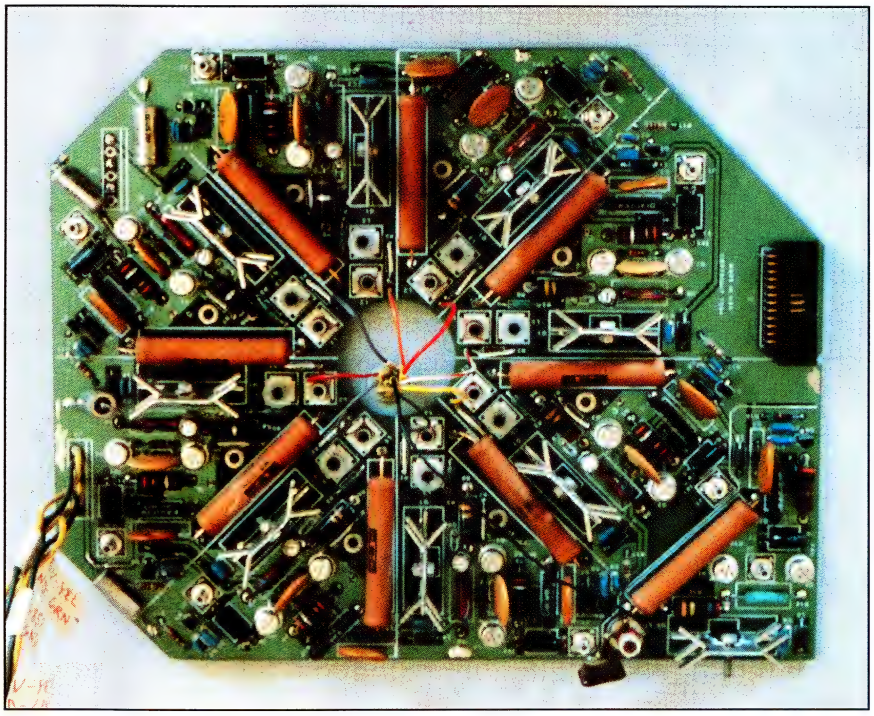
EIGHT BEAMS PAINT A CRT IMAGE THAT HAS THE DETAIL OF FILM

UNIQUE ELECTRON OPTICS CONTROL INTERACTIVE DISPLAY

An eight-beam cathode-ray-tube raster display with the resolution of photographic film promises new capabilities for industrial, medical, and military imaging systems. The Azuray 2000 uses standard components to drive a 2,048-by-2,048-pixel array by generating a bundle of thin beams, similar to a "brush" of parallel streams of electrons moving at the same 15-kHz sweep rate used in conventional TV. Azuray Inc., Scotts Valley, Calif., has eliminated the switching and control at high data rates required by high-resolution CRTs.

Computerized imaging techniques have made it possible to change individual elements of an image to display it in any desired form. The resolution of computer displays, however, has trailed that of film, which has little or no interactive capability. Thus users have had to make a tradeoff between resolution and the ability to interact with an image.

The Azuray 2000 solves that problem. It can provide many different views of a single image, without time delays or extra cost. An image can be highlighted, altered, sectioned, or enlarged. Areas of interest can be expanded and examined in detail. The image can even be manipulated to display more detail than the original film showed.



1. 8-WAY DRIVE. The Azuray 2000's video board has eight amplifiers—one for each beam.

Some of the more promising applications for the 2000 are in oil exploration, military intelligence, and medical diagnosis. In oil exploration, for example, the image can provide electronic pictures of geologic strata for oil companies trying to locate small deposits. Military-intelligence organizations could use the system to develop flexible and easy-to-transmit displays of satellite images, which could then be sent instantaneously to commanders in distant locations.

High-resolution electronic imaging portends dramatic changes in how doctors make diagnoses. For example, not only can a patient's X rays be kept on line for instant retrieval but they can also be selectively enhanced to bring out particular areas in real time. This is an advantage that film does not have. Medical specialists—even when far removed from the site of an examination—would have detailed images upon which to base an informed diagnosis. The Azuray 2000 has already been incorporated in a medical-diagnosis system from Matrix Instruments Inc., Orangeburg, N. Y., that can digitize X-ray film for electronic analysis.

The high-resolution image displays currently in use provide a picture definition of roughly 1,280 by 1,024 pixels. But even conventional CRTs can potentially resolve up to 5,000 lines—which means a much higher pixel density. The problem in building high-resolution devices, however, has been in coping with their high data-handling and beam-steering requirements: for a single beam to paint 5,000 lines 60 times a second, video bandwidths of up to 300 MHz and horizontal deflection frequencies of 120 kHz are required. In addition, digital data must be converted to analog signals at the video frequency, and deflection waveforms must be generated at the deflection frequency.

Azuray's approach was to exploit the potentially high resolution of CRTs by using a parallel array of beams, avoiding the switching and power requirements that would be needed to illuminate them with conventional video circuitry. A parallel-beam display that would cut switching and bandwidth requirements by two thirds could be built from a conventional three-color shadow-mask gun operating monochromatically.

However, shadow-mask tubes use wider beams—about 0.025 in. in diameter, or five times wider than required for high resolution. Even if shadow masks could be made fine enough, they would be so thin and fragile that they would be vulnerable to damage from the high beam-deflection cur-

TECHNOLOGY TO WATCH *is a regular feature of* Electronics *that provides readers with exclusive, in-depth reports on important technical innovations from companies around the world. It covers significant technology, processes, and developments incorporated in major new products.*

rents. The 2000 does not use a shadow mask. Instead, it steers many thin beams—about 0.003 in. in diameter—thereby reducing the system's requirements for high beam-deflection currents.

The basis of the Azuray system is the multiple-beam approach developed by Arthur J. Rank Industries, a British designer and manufacturer of CRTs, according to Roy Murphy, vice president of research and development, who helped design the 2000. Rank developed a 12-beam tube that builds pictures a line at a time on film that is pulled across the faceplate. The technology was used originally in a military application by Honeywell Inc. for its AAD-5 airborne infrared reconnaissance system. Azuray adapted Rank's multiple-beam technology and added the ability to deflect the bundle of beams to create a raster display.

Azuray's approach uses a commercially available 17-in., 70° tube using P45 phosphor. The Azuray 2000 uses a 25-kV anode voltage with a single-channel bandwidth of 50 MHz and conventional sweep frequency to obtain a system bandwidth equivalent to 400 MHz.

UNIQUE SYSTEM

To achieve this performance, the 2000 uses a unique system of electron optics to generate, deflect, and control its eight independently addressable beams. All eight beams are produced from a single cathode, which generates electrons that pass through a grid stack, a laminated structure consisting of five conducting layers separated by four insulating layers. The intensity of the individual beams is regulated by eight video amplifiers in a control grid (Fig. 1).

The information to control the beams requires a dedicated processor with its own memory, plus image memory, graphics- and video-control circuitry, and digital-to-analog converters for each beam. Each pixel requires 8 bits of image memory to provide a 256-level gray scale. The basic Azuray system thus uses 8 megabytes of image memory to provide two complete 2-by-2-K images—one for data and one as an overlay for grids, vectors, or alphanumeric data—that can be displayed simultaneously. Up to 64 megabytes of memory and 16 images can be accommodated.

Azuray uses 120-ns dynamic random-access memory, which is dual-ported to allow simultaneous access by the central processing unit for pixel addressing and by the video controller to switch the beams through the grid stack. The stack contains an array of 0.007-in. holes in two parallel staggered rows. There is a 2-pixel pitch between any two elements of a row and 3-pixel separation between the rows. Delaying the leading row by 3 pixels during a sweep produces a linear row with a 1-pixel pitch at the screen.

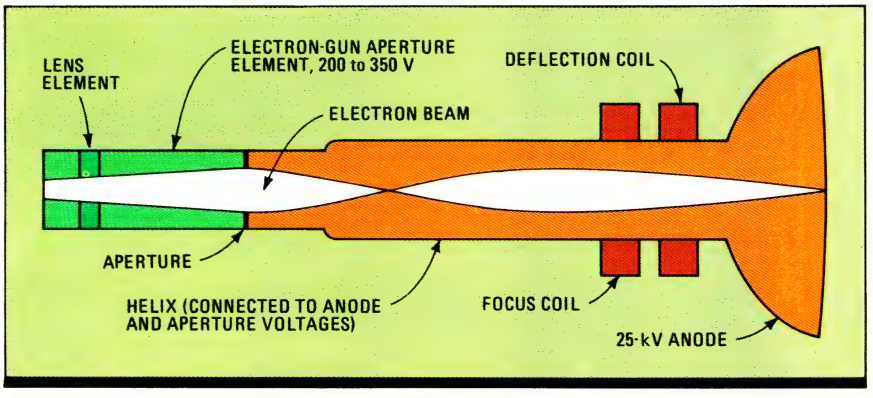
DRIFT SPACE

When the beams emerge from the stack, they enter what is essentially a drift space, at the end of which is a 0.12-in.-diameter aperture. The aperture's dimensions represent a fairly wide opening for what is to become a high-resolution beam bundle, but the electron divergence from the grid stack is substantially greater. Thus the aperture can intercept about 90% of the initial beam current.

After the aperture, the beams pass through a strong electrostatic lens formed by the end field of the helix, a resistive 250-MΩ structure between the aperture and the anode. Additional focusing at this point shapes the beam as it travels down the tube (Fig. 2).

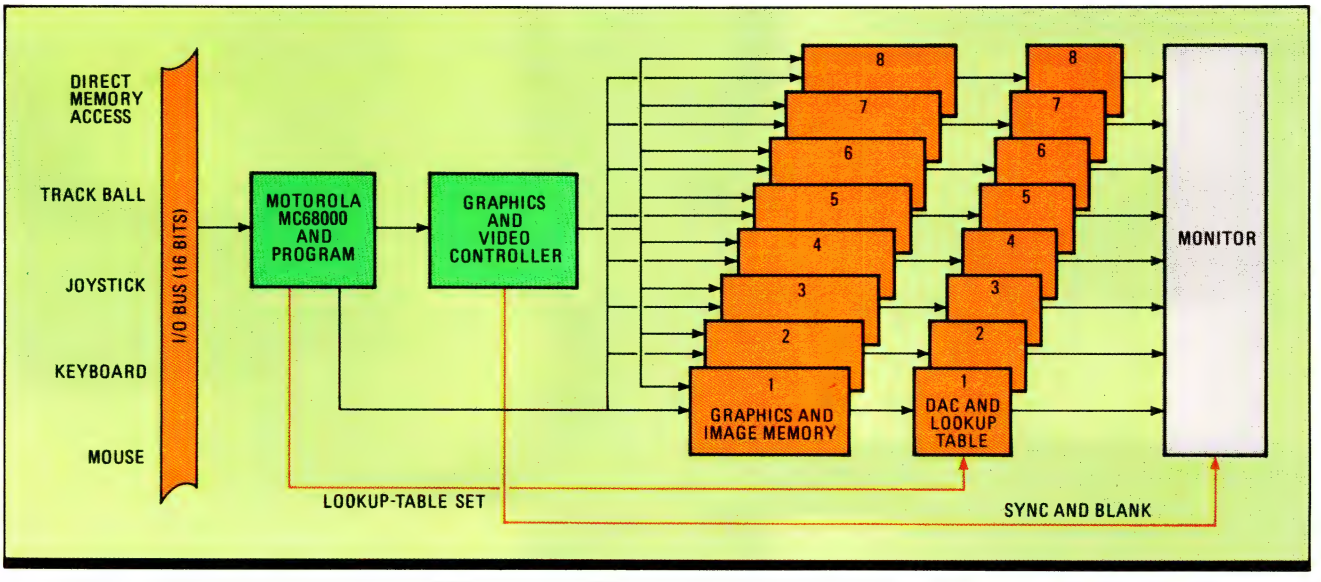
The beam bundle undergoes one crossover at the control grid about an inch ahead of the end of the gun. Then, under the action of the helix, the beams become increasingly collimated. An electromagnetic lens field causes a second crossover to occur at the end of the helix, which produces the final focus at the screen. The last element in the chain is the deflection coil, which is a conventional stator-wound design.

The size of the beam at the screen is actually an image of the first crossover,



2. BEAM STEERING. The CRT (left) uses a raster scan that sweeps the screen in a beam of parallel lines, forming the picture.

3. TRAFFIC COP. The microprocessor (below) directs address data and control signals between the graphics and the video systems.



where the beams are much smaller than a pixel. Actual measurements show screen spot size to be on the order of half a pixel, indicating that systems with four times the resolution (4-K by 4-K) are feasible.

A color version of the display, using the Tektronix Inc. liquid-crystal shutter to obtain color from white light, is also available [*Electronics Week*, May 6, 1985, p. 18]; and 4-by-4-K displays are possible using the same technology.

DIVISION OF LABOR

The microprocessor, a Motorola Inc. 68000, directs data and control signals between the image memory, address, and a graphics and video controller. The dual-ported image memory can simultaneously provide storage for each beam and allow the CPU access to any pixel in an image frame. CPU memory requests are delayed if they coincide with video-display-processor-memory requests.

The memory is organized in three-dimensional chunks called tiles, which measure 16 bits horizontally, 8 bits vertically (1 bit for each beam), and 8 bits deep (for the gray scale). All bits in each tile are fetched in a single memory cycle; the CPU can address any pixel on the surface.

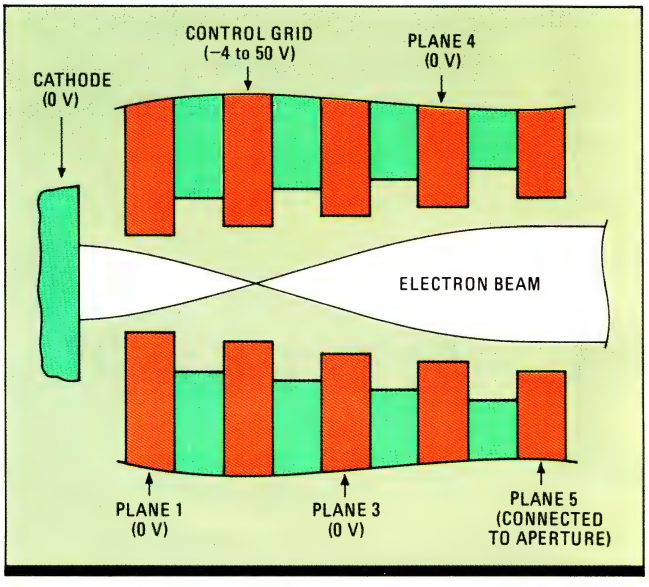
The video signals, one for each beam, are generated by eight DACs of 8 bits each. Ordinarily, the output level of each DAC is a fraction of its 55-V reference voltage determined by the 8-bit input. However, when the overlay image generates a signal, the DAC output is the entire 55 V, overriding any signal from the main image.

The video ports of the memory controller thus have priority over requests from the CPU ports, and the video-display processor has priority access to the image memory while the CRT monitor is scanning. The CPU ports are used to read and update the image and overlay memories, which must be generated in lock-step with the scan position of the beams.

Luminosity data for the image is provided by eight lookup tables located between the image memory and the digital to analog converters (Fig. 3). These tables can be controlled dynamically by the CPU. The tables allow changes in screen intensity to make different portions of an image visible. The user can effect these changes by means of a keyboard, joystick, trackball, or mouse, or from a host computer over a DMA link. Communications interfaces include Unibus, Q-bus, and VMEbus.

These digital controls ensure that the beam brush arrives at the tube perfectly aligned and at the correct luminosity.

4. IN FOCUS. The eight-beam bundle goes through a crossover point halfway down the tube. The bundle is focused by an electrostatic lens.



TRIO FOCUSED ON IMAGER'S DESIGN

The design of the Azuray 2000 is mainly the work of three company executives: Roy E. Murphy, vice president of research and development; Robert S. Lau, vice president of engineering; and Robert G. Quick Jr., director of tube engineering.

Murphy, who holds a PhD from Stanford University and an MSEE from the University of Connecticut, has spent 35 years in engineering and software-systems development for image processing.

Both he and Lau have directed technical projects at the Acoustic Research Center. Lau has a BSEE from the University of Minnesota and an MSEE from the University of California at Berkeley.

Quick, the original designer of the multibeam tube, has worked as a designer at the Rank America tube division and with Litton Electron Devices. He holds a dual degree in chemistry and chemical engineering from Syracuse University. His work at Azuray led to the patenting of its imaging system.

ROY E. MURPHY

Because the tube's faceplate is much flatter than it is spherical, however, the image must be corrected for focus and astigmatism at the corners. The raster scan, for instance, is wider at the corners than at the center, a condition that can be corrected partly by improving the deflection-yoke design but that also requires mixing horizontal and vertical deflection signals.

Focus at the table's corners is controlled by an extra winding to the focus coil, which can be driven dynamically to change the focus of the electromagnetic lens (Fig. 4). A commercially available astigmatism coil can correct any astigmatism. The correction current differs for each tube, however, according to both the placing of the coil and the characteristics of the tube.

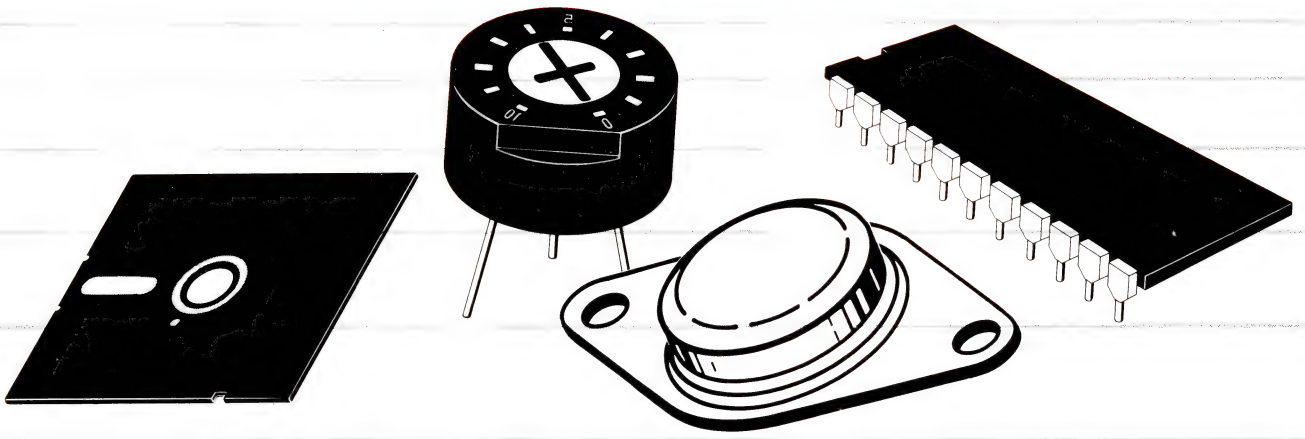
TUNED INDIVIDUALLY

After attempting to design analog deflection techniques to account for any variation, Murphy chose instead to tune each tube and then store the required correction in an erasable programmable read-only memory. Other second-order aberrations, such as twist and size variation, result from the interaction of the other coils. Twist can be corrected by a solenoid coil around the neck of the tube. But again, this correction varies from tube to tube and is highly dependent on the position of the other coils. Spot size is affected by voltage to the lens element, although the correction waveform has not yet been reduced to an equation.

Because the apparent resolution of this type of CRT is so much better than the minimum 2,048 by 2,048 pixels required for the applications that Azuray envisions, the company expects it will be relatively easy to develop tubes of even greater resolution by increasing the number of beams. And because each beam is driven by a signal that resembles conventional TV formats, the Azuray system could be adapted to transmit high-resolution 2-K-by-2-K medical images anywhere in the world, using eight TV channels. □

The industry's leading coverage of technology news.

In Electronics.



Electronics is back–with the industry's best reporting on technology. In the first half of 1985 alone, Electronics featured hundreds of important articles with news and analysis that leaders in the field can't afford to be without:

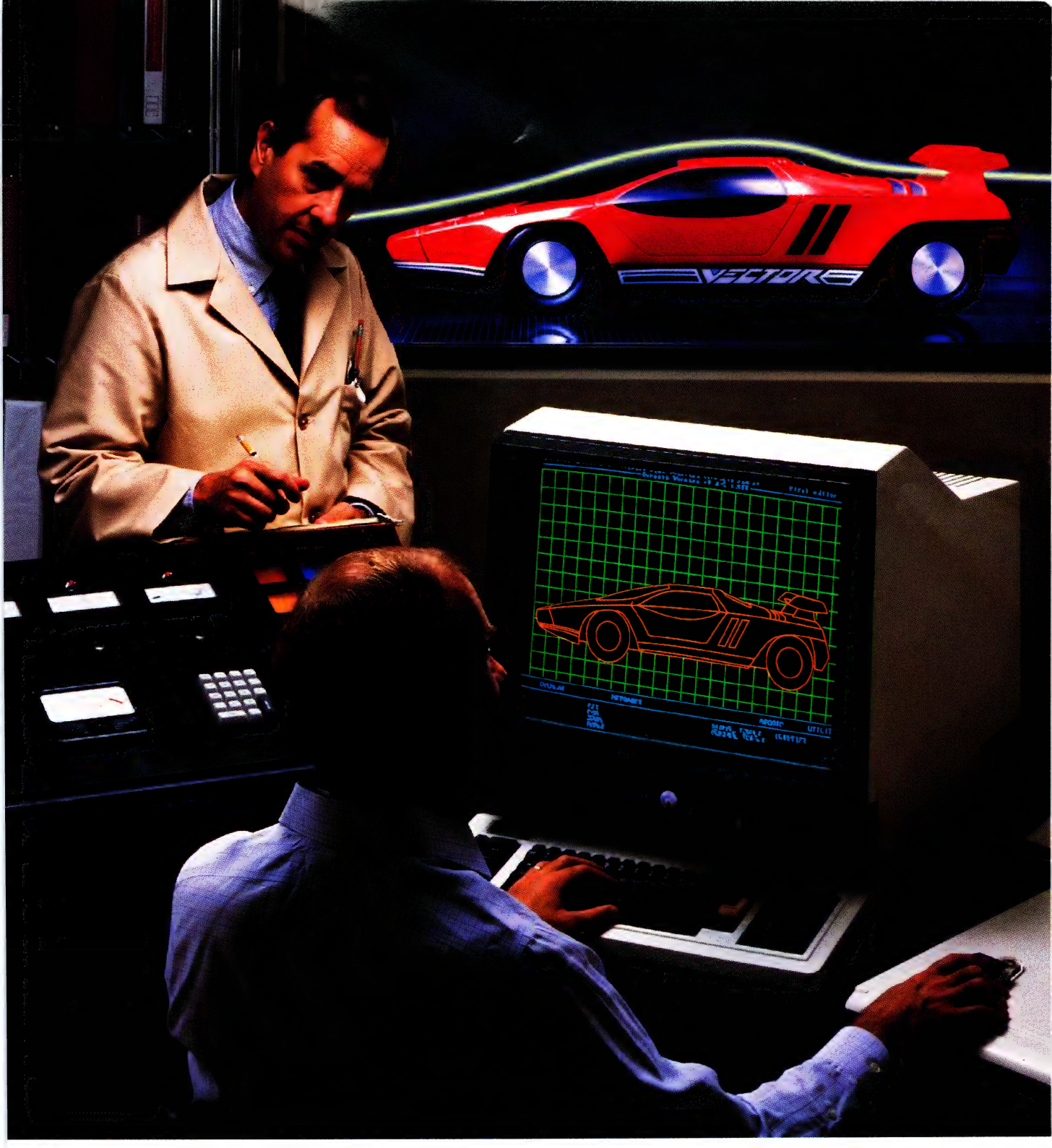
- Full coverage of computer technology, with 86 articles on computer systems, 50 on software, 33 on boards and peripherals, and 28 on CAD/CAM
- 140 articles on international technology
- 30 articles on military technology
- 27 articles on the latest developments in test and measurement equipment
- Over 100 articles on communications technology
- 40 articles on components technology
- More than 100 articles on worldwide events in semi-conductor technology.

Readers depend on us for this full scope of technology coverage worldwide. Shouldn't your selling message be in Electronics' environment of pivotal technology reporting and analysis?

Put your advertising where the electronics attention is. Call Electronics today, at 212/512-3140 (U.S.), to reserve your ad space. Outside the U.S. contact your sales representative.

Electronics is back. Shouldn't you be back as well?

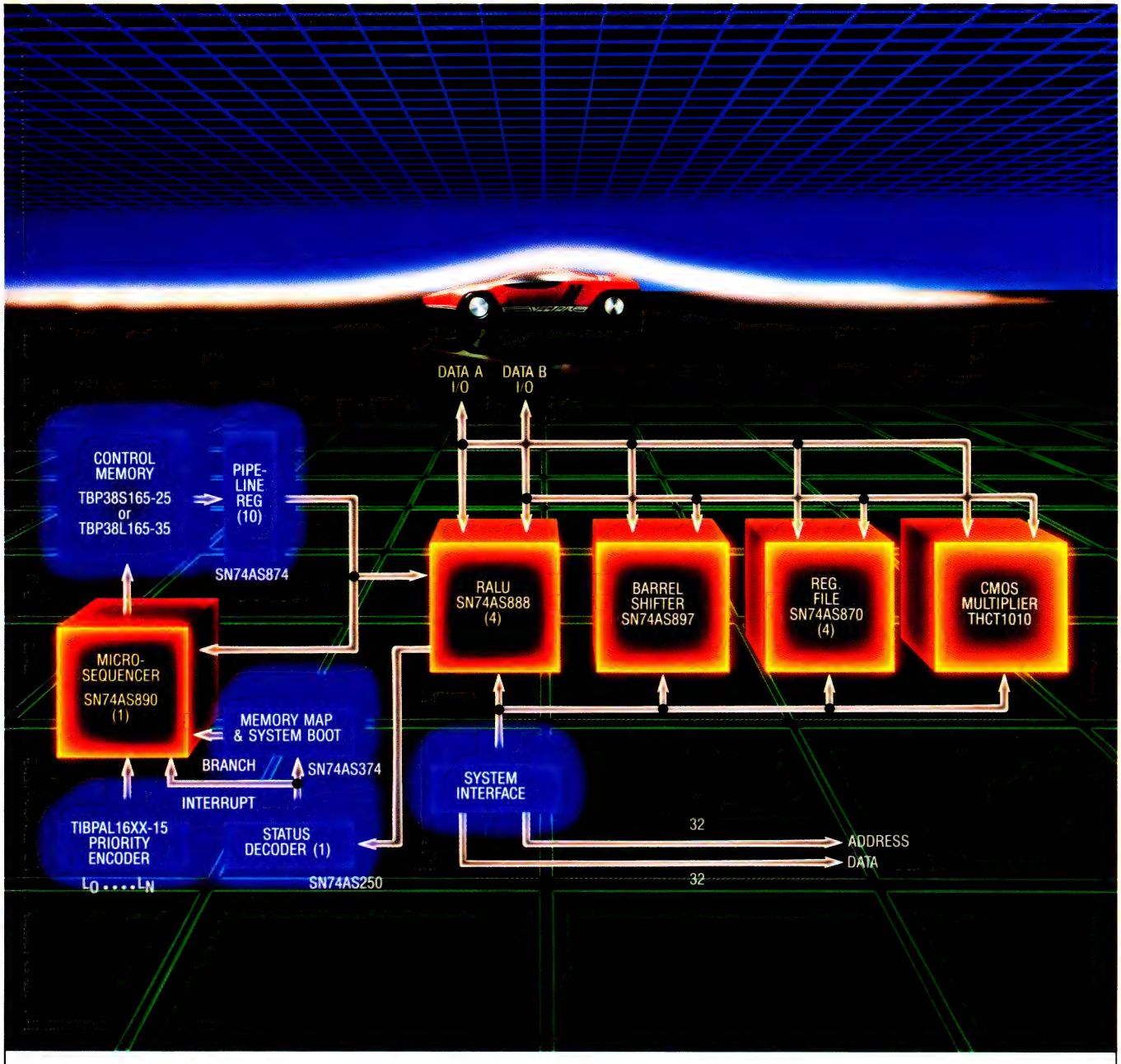
McGraw Hill



Design for faster system performance with new IMPACT 8-bit-slice processor from Texas Instruments.

- **Outstanding speed,** low power, and flexibility of TI's advanced 74AS888 processor boost system throughput (*page 2*).
- **Cost-effective digital control** is provided by TI's single-chip, high-speed TMS32010 signal processor (*page 3*).
- **Dramatic savings in system power** are achieved using TI's new CMOS THCT1010 multiplier/accumulator (*page 4*). ▶

TI's innovative 74AS888 processo



Substantial throughput improvements result when four of TI's new 74AS888 8-bit-slice processors are cascaded to create a high-performance 32-bit CPU. The 74AS888 will enable next-generation work stations and graphics systems to record and manipulate data with significantly greater efficiency.

For applications where speed is your driving force, there is a new way to maximize system performance. TI's 74AS888 IMPACT™ 8-bit-slice processor. Use it to upgrade present bit-slice-based designs. Use it in next-generation digital computers and controllers, disk-drive controllers, high-resolution graphics systems, and array processors.

The 74AS888-1 offers an instruction-to-Y output of 46 ns maximum. That's a 51% improvement over the 4-bit competition. And power dissipation is only 1.5 W maximum during operation (*see graph at right*).

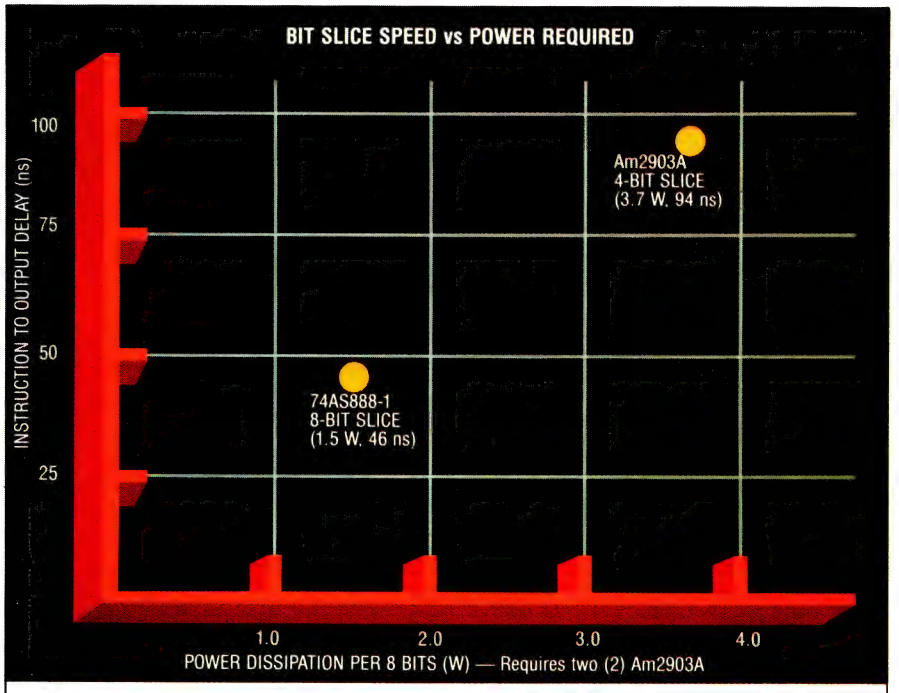
Superfast multiplies and divides

That's because TI's 74AS888 has unique on-chip overflow detection and ALU bypass. Also, three separate I/O paths allow simultaneous fetching of operands, execution, shifting, and storing of results without arbitration. And the three-operand register file can combine an operation and a move instruction in a single clock cycle.

The 74AS888 has full on-chip decoding and on-chip binary conversion to BCD, single- and double-length accumulators for double-precision answers, and an edge-triggered register file to simplify system design.

™Trademark of Texas Instruments Incorporated

delivers 51% greater throughput.



Impressive speed/power performance is possible by using TI's new 74AS888 processors. 0.8-ns internal-gate switching and 100-μW internal-gate power dissipation contribute to the 51% speed improvement of the 74AS888-1 as measured by instruction-to-output delay. Power is reduced by 60%. The unique IMPACT (Implanted Advanced Composed Technology) process developed by TI is used to fabricate the 74AS888 processors. IMPACT techniques include oxide isolation and composed reticles to achieve 2-micron geometries essential to the development of advanced VLSI products.

Flexible instructions for complex math

Fixed instruction sets limit the kind of operations a microprocessor can be programmed to do. But you program the 74AS888 using a comprehensive set of microinstructions — 13 arithmetic and logic functions, 8 single- and double-length conditional shifts for magnitude scaling, and a wide range of bit-, byte-, and word-manipulation instructions. With TI's 74AS888 you can tailor an instruction set precisely to your application. Use any software. Use any word length in 8-bit increments. Even emulate any known μP instruction set, achieving substantial improvements in system throughput.

High-speed 74AS890 microcontroller supports symmetrical pipelining

Microcoded instructions are stored separately from main memory, generally in a high-speed PROM or static RAM. Handling the sequencing and batching operations between this storage space and the 74AS888 is TI's high-speed 74AS890. It is a 14-bit microinstruction controller that can address up to 16K of control-store memory. The 74AS890 can also serve as a powerful, stand-alone sequential controller.

The 74AS890 can perform 16-way branch operations, realtime interrupts, and nondestructive reads of a nine-word-deep stack. Two 14-bit counters can be used for nested-loop operations. The maximum clock-to-output delay of 42 ns for the 74AS890-1 balances the memory microcycle timing with the 74AS888-1 data-execution timing cycle.

Space-saving, economical packages

Now available from TI distributors in a 68-pin ceramic grid array, the 74AS888 and 74AS890 will soon be available in a 68-pin plastic leaded chip carrier. Both packages are offered at the same price. Military versions will be available in leadless ceramic chip carriers.

The price of the 74AS888-1 is $166.00 and that for the 74AS890-1 is $87.00, in 100-piece quantities each. The price will decrease according to high-volume purchase commitments.

TI's single-chip DSPs with 200-ns cycle time: Low-cost solution to high-speed control.

An extremely effective alternative for improving system performance is TI's TMS32010 Digital Signal Processor, which can be applied in high-speed-controller applications where digital control replaces analog servo-loop processing. Having a high degree of integration and an outstanding combination of features, the TMS32010 is very cost-effective (1) as an application-specific controller in existing bit-slice designs or (2) as a stand-alone controller handling the multiple functions often required by a single application.

For example, the TMS32010 could enable an industrial robot to perform mechanical operations through digital/servo-loop computations, to synthesize and recognize speech, and to sense objects with radar or optical intelligence.

Having a 200-ns instruction cycle, the TMS32010 gives you the flexibility of a high-speed controller and the numerical capability of an array processor in a single 40-pin DIP. The TMS32010 contains on-chip data RAM, on-chip program ROM, a 32-bit ALU/accumulator, a 16 × 16-bit parallel multiplier, and a barrel shifter.

Seven TMS32010 Application Notes, including one entitled *Control System Compensation and Implementation,* are available. For the set, send us the coupon from page 4. ■

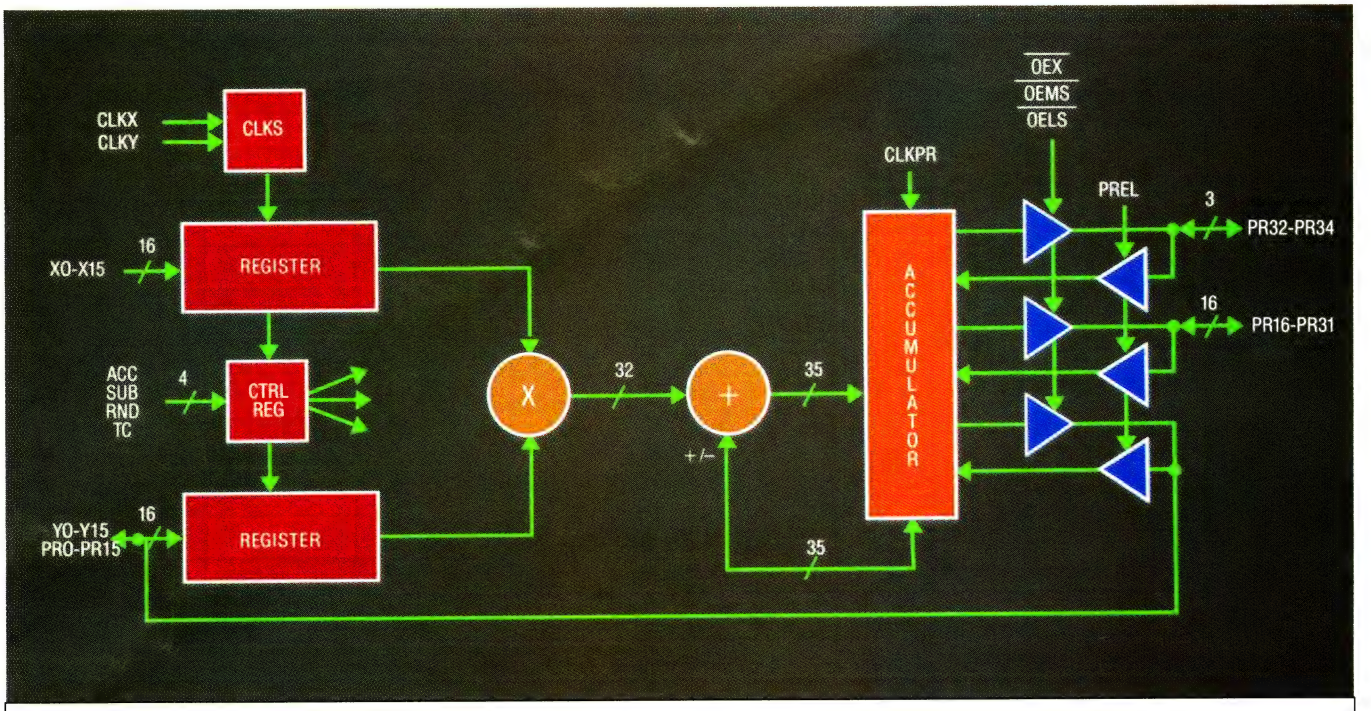
Extensive support

Third-party development support is in place and ready to help you with your implementation of 74AS888 bit-slice systems designs.

If you have questions, a call to **(214) 995-4720** puts you in touch with TI's applications support group. Your nearest TI Regional Technology Center can also answer your questions and tell you about future 74AS888 training courses.

For more information on the 74AS888 and 74AS890, clip and complete the coupon on page 4. ■

Turn page for more information.



TI's new THCT1010 16 × 16-bit multiplier with 35-bit accumulator consumes one-thirtieth the power of equivalent devices.

New TI CMOS multiplier/accumulator can slash bit-slice system power.

Pin-for-pin compatible with the industry-standard TDC1010J multiplier, TI's THCT1010 consumes 30× less power. In conjunction with TI's new low-power 74AS888 processor, it can significantly cut the power requirements of bit-slice systems.

Fabricated in silicon-gate CMOS, the THCT1010 is a 16 × 16-bit multiplier with 35-bit accumulator (*see diagram above*). How fast is it? For the -100 suffix, 100 ns maximum with a typical power consumption of only 150 mW.

Contributing to this remarkable performance are twin-well processing, a modified Booth's algorithm, feed-forward carry circuit, and conditional sum adder. TI's new THCT1010 performs multiplication and addition, multiplication and subtraction, and straight multiplication. Output can be rounded to the 19 most significant bits and formatted in two's complement or unsigned magnitude.

Such programmable features fit the THCT1010 for digital signal processing, digital filters, fast Fourier transforms, array processing, graphics calculations, and microprocessor-throughput enhancement.

For more details on the two THCT1010s available, return the coupon. The THCT1010-100JD offers the 100-ns multiply/accumulate time across a 0°C to 70°C temperature range; the THCT1010-140JDE operates over an extended −60°C to 85°C at 140 ns. Both are available in 64-pin ceramic DIPs (JD), and will soon be available in 68-pin plastic chip carriers (FK). ■

©1985 TI

27-5274

Texas Instruments Incorporated
P.O. Box 809066
Dallas, Texas 75380-9066

SDB013EC500C
Expires June 30, 1986

I like what I've read; send me more:

DB01 ☐ IMPACT 74AS888 8-bit-slice processor and 74AS890 high-speed microcontroller
PR22 ☐ TMS32010 DSP microcomputer Application Notes
CL04 ☐ THCT1010 CMOS multiplier/accumulator
☐ I have an immediate application; please have a Field Sales Engineer call on me.

NAME

TITLE

COMPANY

ADDRESS MAIL STATION

CITY STATE ZIP

AREA CODE TELEPHONE EXT.

TEXAS INSTRUMENTS
Creating useful products and services for you.

MINISUPERCOMPUTER DIVIDES TO CONQUER

SEPARATE MATH PROCESSORS BLAZE THROUGH CALCULATIONS

Making advances in circuit technology and packaging are obvious ways to speed up computers. Using available parts to come up with innovative architecture is less apparent and perhaps more demanding. Glen Culler, chairman and principal system designer at Culler Scientific Systems Corp., took this path to design and develop the Santa Barbara, Calif., company's newest minisupercomputer. The Culler 7 is based on a distributed-function, highly concurrent architecture with a strong emphasis on mathematical calculations.

The design represents a major advance in scientific computer architectures in two ways. First, it separates mathematical calculations from the operating system's managerial functions. Second, it has a built-in mathematical bias in the computational processor's design. The modular system can contain from one to four of the special-purpose 64-bit computational processors and a 32-bit operating-system kernel processor.

Designed for heavy-duty arithmetic, the user processors have an internal parallel-processing structure, use large amounts of cache in nontraditional ways, and have mathematical functions that are frequently used by scientific programs built into the hardware and microcode. Each processor performs several functions during a clock cycle. The 32-bit kernel processor handles the system operation, which involves many short tasks and frequent context switches. The operating-system software executed by the kernel processor is based on the 4.2bsd version of AT&T Co.'s Unix from the University of California, Berkeley. A common back-end compiler optimizes concurrency in both scalar and vector processing for front-end Fortran 77 and C language compilers.

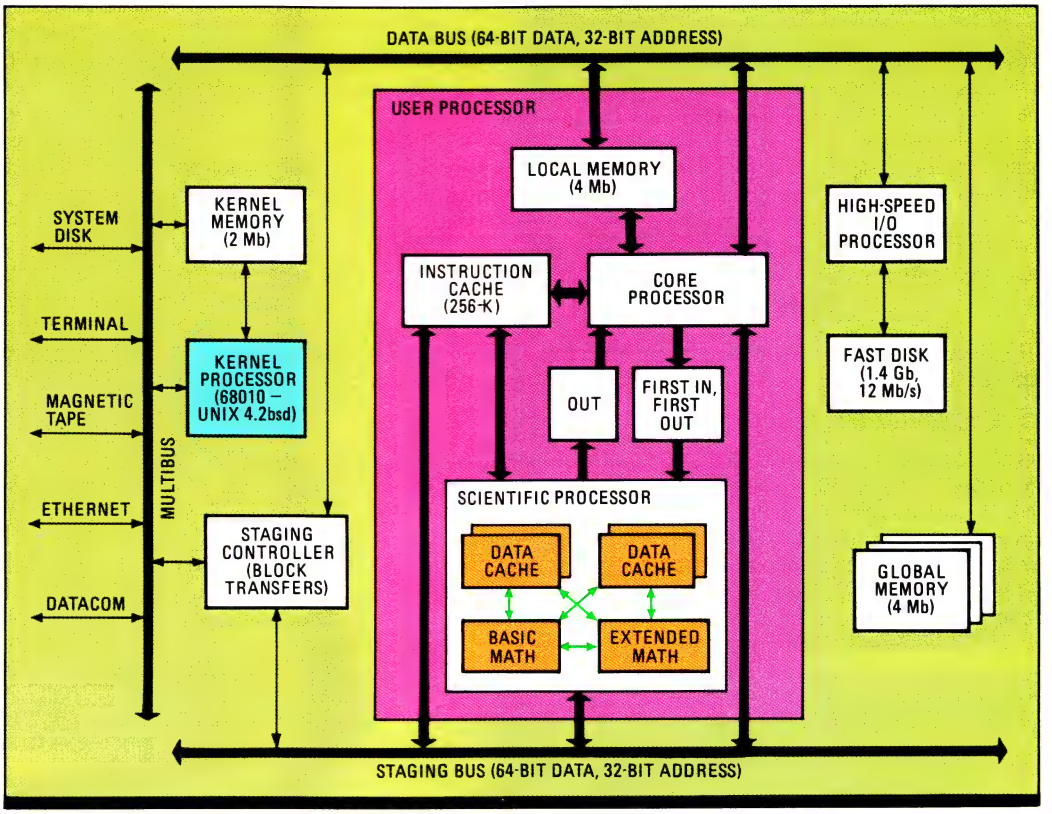
The low end of the six models in the Culler 7 family perform 7 million instructions per second and 2 million floating-point operations per second in a computation server for work-station networks. A five-processor model executes 36 mips and 16 megaflops. Prices range from less than $250,000 to under $1 million.

The Culler 7 owes its speed to a combination of the best features from general-purpose and vector-processing scientific computers. Scientific applications tend to blend integer and array processing to solve problems. Most superminicomputers on the market are general-purpose and do not perform floating-point calculations quickly. And the vector-processing supercomputers and array processors attached to superminicomputers and mainframes cannot handle unpredictable program flows and integer calculations very well.

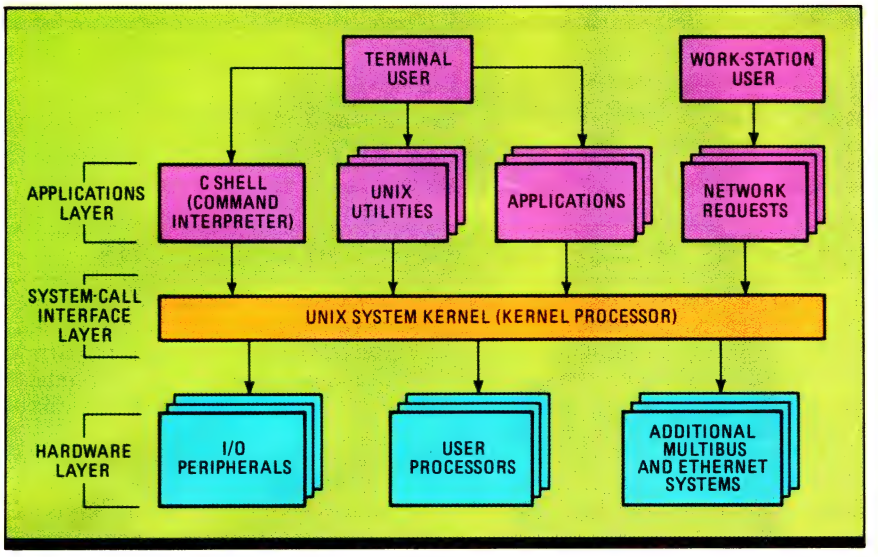
The Culler team's design goal was to maximize the speed of both vector and nonvector processing. The design had to be as resistant as possible to the performance-degrading effects of mixed calculation types and nondeterministic program flows. In addition, the team aimed to give the average scientific user the ability to write efficient programs at the Fortran and C programming language levels—eliminating the need to resort to machine language to wring out more speed. To achieve the second goal, the designers developed smart compilers that could automatically optimize code for the Culler architecture.

The user processors do the Culler 7's high-speed computations (Fig. 1). They connect to the system through two fast 56-Mb/s data and staging buses. The data bus acts like the main bus of most systems and is used for data movement and communication access. But the staging bus performs a special function. It is used exclusively by a staging controller—a special block-transfer device—for loading tasks to and unloading them from the user processors. Each bus has a 64-bit data part and a 32-bit address section.

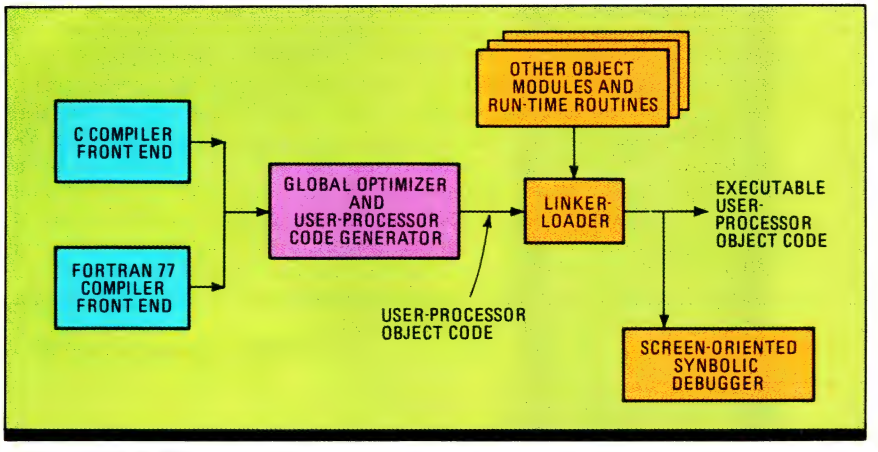
Four basic parts make up the user-processor structure—



1. ELAN VITAL. The lifeblood of the Culler 7 minisupercomputer system is the user processor, with internal math processors, cache memories, a core processor, and local memory. A kernel processor manages the system.



2. LAYERS. The Unix system kernel on the kernel processor controls the software system. It receives code from the application layer and directs it to the appropriate hardware resources.


OTHER OBJECT MODULES AND RUN-TIME ROUTINES
C COMPILER FRONT END
GLOBAL OPTIMIZER AND USER-PROCESSOR CODE GENERATOR
LINKER-LOADER
EXECUTABLE USER-PROCESSOR OBJECT CODE
FORTRAN 77 COMPILER FRONT END
USER-PROCESSOR OBJECT CODE
SCREEN-ORIENTED SYMBOLIC DEBUGGER

3. CODE MAKER. The compiler system centers around a global optimizer and code generator shared by specific high-level language (C and Fortran) front-end compilers.

local memory, instruction cache, core processor, and scientific processor. Within the scientific processor, which executes all scientific calculations, are two tightly coupled mathematics processors—the basic and the extended math processor. The basic math processor handles the more numerous mathematical functions—including addition, subtraction, shifts, data-type conversions, bit and byte manipulations, and logical operations such as AND, OR, and XOR. It does integer and single-precision calculations in one cycle, double-precision types in two.

EXTENDED MATH PROCESSOR

The extended math processor handles all multiplication and division, both integer and floating point, as well as microcoded math functions, such as the standard trigonometric functions, square root, and the like. The extended math processor can execute complex instructions needing several machine cycles—double-precision floating-point divides, for example—while the basic math and core processors execute other instructions in parallel. Also, because of the very tight coupling between them, the extended math processor can direct the basic math processor to help it execute parts of complex multicycle operations, such as fast Fourier transforms and matrix-dot products.

In addition to being tightly coupled to each other, both math processors are tightly coupled to two data caches at their disposal. The intelligent compilers know about the pair of dual 16-K 45-ns caches and their structure and are able to generate efficient code that uses them for such things as fast program stacks and register files. This makes a very flexible and fast register-and-stack subsystem that can be used to advantage in optimizing jobs that are heavily calculation oriented. The compilers can also select another mode and use this cache pair as fast array memory.

To speed the two math processors' operation, the staging controller loads the dual 32-bit-wide data caches with duplicate blocks of data. The math processors access the data caches by single-location loads and stores. The math processors cannot directly access the local memory in the scientific processor nor the global system memory. Instead, the core processor handles that.

The input-data transfer mechanism between the core processor and the math processors is the 64-bit-wide, 3-word-deep first-in first-out buffer. This provides flexibility and overlap in data movements. The core processor can race ahead to acquire the next three data items, for example, while the math processors are busy crunching on the last one. Then, when the math processors crunch the next three data items, the core processor could execute sequence-control instructions or basic integer math operations. The output-data transfer mechanism, for results from the math processors headed for main-memory storage, uses a single-stage output buffer between the scientific processor and the core processor.

The 32-bit core processor inside the user processor is in charge of many activities to allow the scientific processor to concentrate on calculations. The core processor computes addresses, fetches data from and stores it into local and global memories, manages program-flow through branches and subroutine and system calls, as well as helping the scientific processor on some basic arithmetic functions. The compilers make the arithmetic load-balancing decisions.

The core processor executes all its instructions in one cycle and has access to two 32-bit register files—16 general and 17 special-purpose registers. Both the core processor and the scientific processor get their instructions from the fast instruction cache, which is loaded by the staging controller.

The high-speed instruction-cache memory is a holding tank for instructions that are en route to the core and scientific processors. It has 256-K of 128-ns memory. Instructions come from the staging controller by way of the staging bus. The instruction cache delivers two concurrent streams of instructions to its processors.

The system also handles other memories. One is the dual-ported 4-Mb local memory in each user processor. To minimize the throughput load on the system bus, access to this local memory by the user processor's internal processors is through a separate 56-Mb/s private bus. One local-memory port connects to this internal port, the other to the system's data bus.

The large shared global memory also connects to the system data bus. Because all local memories are also accessible to any user processor, the only difference between local and global memory is that the former have the high-speed private bus link to their core processor to increase the overall system

memory bandwidth. This memory-system configuration mandates that software—the compilers—takes this structure into account and keeps local programs and data in local memory, leaving the global memory for input/output, shared data, and interprocessor communications whenever possible.

Also outside of the user processors at the system level, like the global memory, is the kernel processor, with its own 2-Mb kernel memory. The kernel processor is the operating-system processor for the entire system. It is based on a Sun 2 processor and memory board from Sun Microsystems Inc. that incorporates the Motorola 68010 and attaches to I/O peripherals, terminals, and work stations through a standard Multibus. The kernel processor, running the Unix 4.2bsd operating-system code, deals with the other processors—user processors and the high-speed I/O processors—through a task-control and interrupt mechanism.

When the kernel processor initiates a task in another processor, it fills out a task-control block specifying the task, its size in bytes, and its starting address, plus additional information as needed. Then the kernel processor sends an interrupt signal to the staging controller so it can take the task-control block, attach an order to begin executing the task behind it, and then send the task and the start order into the appropriate processor—loading it into the instruction cache of a user processor, for example.

The staging controller is the system's manager. This special block-transfer device ensures that the right blocks of instructions and data get to the right part of the system at the right time with all the information needed to operate on them. The staging controller has little programmed intelligence, working under the command of the kernel processor.

The staging controller's job is to ensure that all user processors have two tasks at hand—the task currently running and the next one to run. It also removes the results of finished tasks and sends them to the global memory. The staging controller and kernel processor allow the user processors to run flat-out all the time.

The operating-system software directs all management and scheduling of system resources. In the Culler 7 system, the Unix system kernel running in the Sun 2 kernel processor is the system-call layer—the middle layer—of a three-layer operating-system structure (Fig. 2). The upper, or applications, layer contains all the Unix utilities and the high-level language applications; it also receives all network requests and interprets C commands. The lower layer is the hardware.

Unix 4.2bsd was designed to run a single-processor computer system. For the Culler 7, it has been converted to run a complex multiprocessor system with several levels of memory. But at the same time, it remains compatible with the standard version and transparent to users, so they can program and work in an environment that appears to be standard monolithic Unix. Underneath this calm surface, however, Culler 7 Unix is anything but monolithic. Its main job is distributing software tasks among many processors and I/O subsystems.

Culler modified Unix 4.2bsd in several ways to take advantage of the architecture. It increased the disk file block size from 2- to 8-K, which speeds up disk transfers. Many internal exception-processing tasks, such as divide-by-zero, floating-point exceptions, and memory-management faults, are distributed to the user processors. And a round-robin selection assigns tasks to multiple user processors to help spread the workload evenly.

One of the most innovative aspects of the Culler approach to maximizing instruction throughput are the concepts applied to the language compilers. Instead of using costly and complex hardware preprocessors to divide the program code among specialized coprocessors and adding postprocessors to combine the results, the Culler system relies on smart compilers that make all parallel-expansion decisions at compile time. The compiler can easily contain more complex logic than hardware, and the cost of manufacturing volumes of written and debugged compilers is trivial compared with that of making copies of hardware preprocessors, coprocessors, and postprocessors. This approach thus introduces lower manufacturing cost, besides very intelligent structuring of programs for parallel processing.

The compiler structure includes several front-end language processors, one for each language handled (initially C and Fortran 77), connected to a common back-end optimizing code generator (Fig. 3). The optimizing code generator uses modern optimizing techniques such as flow analysis, low-level common subexpression elimination, folding and propagation of constants, dead-storage elimination, register allocation by lifetime analysis, loop optimization, and user-processor optimization.

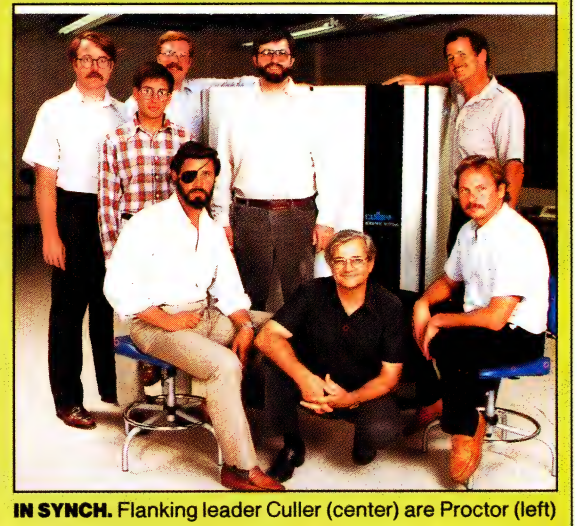
User-process optimization attempts to make the most efficient use of hardware by rearranging the normal sequence of program execution. Because the user processors can each simultaneously execute a basic math operation such as addition, a complex math operation such as multiplication, and three fetch or store operations from three memories—two data caches plus main memory—the optimizer's object is to rearrange the code to perform one instance of all five operations in every machine cycle, wherever possible and for as long as possible. This can involve calculating parts of a problem out of the normal sequence. An optimizing compiler system such as this one becomes one of the key technologies for efficient parallel processing. □

THE TALENT BEHIND THE CULLER 7

After 16 years of developing array-processor technology and host interfaces, Glen Culler was convinced that a product for commercial rather than custom application could better meet expanding market needs. So he tapped his company, Culler-Harrison Inc., for talent and founded Culler Scientific Systems Corp.

He recruited a team of software and hardware specialists in January 1983, and their efforts came to fruition with the Culler 7 family last month. They held tenaciously to the concept that software and hardware must be designed in lockstep in order for either to work efficiently.

To that end, the technical staff (pictured) was intimately involved in all steps of software and hardware development. Leading the software effort were vice president of software engineering David Probert and software manager David McMillen. Michael McCammon, vice president of hardware engineering, led hardware development. Rounding out the team were Walter Lichtenstein, Bob Pearson, William Proctor, and John Richardson, all PhD scientists from research and educational organizations.



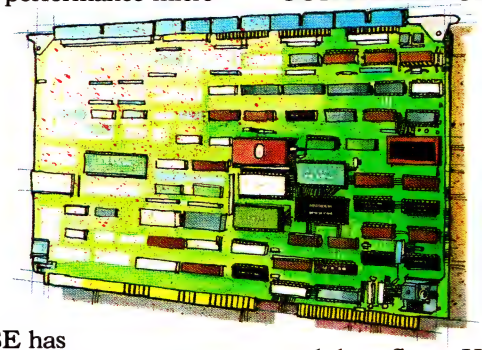
IN SYNCH. Flanking leader Culler (center) are Proctor (left) and Richardson. Members in good standing are (from left) Pearson, Lichtenstein, McMillen, Probert, and McCammon.

WE CAN MAKE YOU THE BIGGEST FASTEST TOUGHEST GUY ON THE BUS TODAY

High Performance Disk, Tape and Communications Controllers, MULTIBUS™ and VMEbus.

When a company says it is going to make you the biggest, fastest, and toughest guy on the bus today, it better be a leader to start with. INTERPHASE Corporation is.

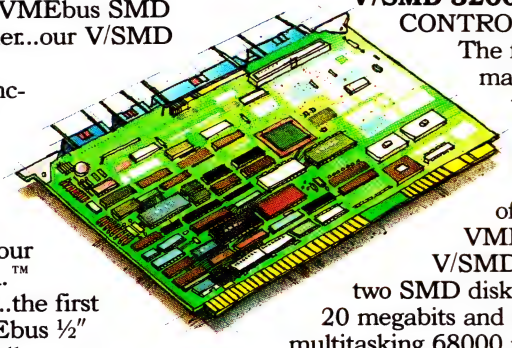
INTERPHASE has more than a decade of leadership in the design and manufacturing of sophisticated, high-speed, high-performance microcomputer products across a spectrum of bus architecture. MULTIBUS, VMEbus, even the IBM® PC bus.



OUR FIRSTS MAKE YOU FIRST

INTERPHASE has always been first-to-market to give *you* the competitive advantage:

- First MULTIBUS SMD disk controller.
- First MULTIBUS SMD controller with CACHING...our SMD 2190.
- First ESDI Winchester controller for ANY bus.
- First multi-tasking disk/tape controller for MULTIBUS...our Storager.™
- First MULTIBUS token passing network controller...our LNC 5180.
- First SMD controller for the IBM® PC...our Maverick.™
- First 32 bit VMEbus SMD disk controller...our V/SMD 3200.
- First full function, single board computer with built-in VMEbus expansion...our BASEboard.™
- AND NOW...the first 32 bit, VMEbus ½" Tape Controller...our V/Tape 3209.



EXCELLENCE BY DESIGN

Our Design Assistance Group will provide immediate support as you first develop your system design, and work with you at every step to completion. And our Applications Engineering Group can save you valuable time and resources as you integrate our high-performance products into your systems.

OUR FAMILY OF PRODUCTS

SMD 2190 MULTIBUS DISK CONTROLLER

Provides your Multibus system with the SMD disk controller power, flexibility and ease of use you need. The SMD 2190 offers such benefits as UNIX™ optimized firmware, intelligent caching, 24 bit DMA addressing and Extended SMD data rates up to 20 megabits.

STORAGER MULTIBUS DISK / TAPE / FLOPPY CONTROLLER

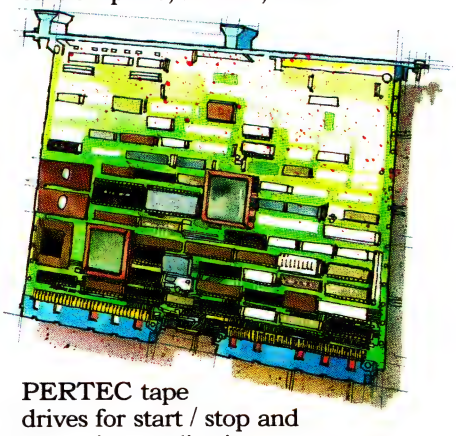
Offers high-performance finesse with force for MULTIBUS on ST506, and ESDI Winchester disks, ¼" tape drives and floppy disks drives. Storager's unique 68000 based Virtual Buffer Architecture speeds up your system by eliminating unnecessary disk latency and allowing concurrent disk / tape operation.

V/SMD 3200 VMEbus DISK CONTROLLER

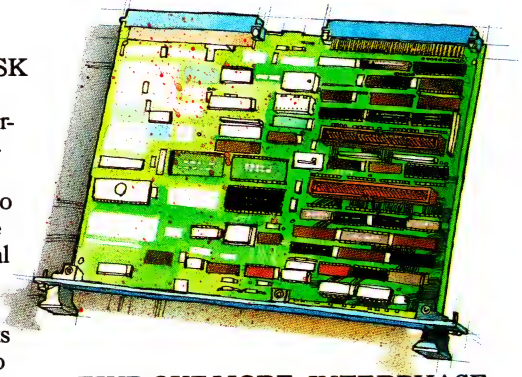
The first high-performance SMD controller which allows you to exploit the full potential of the 32 bit VMEbus. The V/SMD 3200 supports two SMD disk drives at up to 20 megabits and above. Imagine... multitasking 68000 power with Virtual Buffering for UNIX optimized intelligent caching, and zero latency reads and writes. The V/SMD 3200 is the essential element to your VMEbus system performance.

V/TAPE 3209 VMEbus TAPE CONTROLLER

INTERPHASE's latest VMEbus product is a companion to the V/SMD 3200, and opens new VMEbus design options for you. The V/Tape will control up to 8, 9 track , ½ inch



PERTEC tape drives for start / stop and streaming applications. The V/Tape also supports GCR as well as 1600 bpi operations and has ultra fast bus transfer rates at up to 200 ips. Advanced features like 128KB Tape Cache and an on-board 68000 family processor mean it can communicate directly with the INTERPHASE V/SMD 3200 disk controller...cutting your BUS usage in half.



FIND OUT MORE: INTERPHASE is ready to help you get that project up and running...NOW. Call us today to get information about our NO RISK, First Time User Program. (214) 350-9000.

INTERPHASE corporation

2925 Merrell Road • Dallas, Texas 75229 • Telex: 9109976245 NASDAQ-NMS: INPH

MULTIBUS is a trademark of INTEL Corp.
Storager, Maverick and BASEboard are trademarks of INTERPHASE Corporation.
IBM is a registered trademark of International Business Machines.
UNIX is a trademark of AT&T Bell Labs.

Circle 47 on reader service card

BATTLE OF THE BUSES: AND THE WINNER IS...

...VMEBUS, AS MULTIBUS II GETS OFF TO A SLOW START

by Robert Rosenberg

The din was fierce in recent months as major U. S. chip makers fought it out over whose approach was best in 32-bit bus structures. The challenger in the Multibus corner, Intel Corp., was trying to make a big comeback. And Motorola, Signetics, and Mostek were fighting back with VMEbus, the reigning champion. Now the first round in the "battle of the buses" has ended, and the judges have made a decision: VMEbus is the clear-cut winner.

The first wave of boards, built with first-generation 32-bit microprocessor and support chips, is expected to hit the market in volume in 1986. And the number of designers and system integrators who will then build 32-bit VME-based systems for sophisticated process-control systems and advanced engineering work stations is expected to overwhelm those designing products with Multibus-based gear.

VME is riding the crest of its growth curve, taking advantage of its three-year head start on Multibus II. Richard Main, market analyst for Zebu Corp., a Sunnyvale, Calif., market researcher that closely follows the Multibus and VME-board-level market, expects that shipments of VME products will double in 1986 from an estimated $120 million in 1985, then nearly double again, to $450 million, in 1987.

"I changed my long-range projections—last year I thought VME could only do $300 million at the high point of the curve, but now I think it will do $600 million by 1990," Main predicts.

With its 32-bit capability, VME claims the high end of the market for open bus structures—the standardized interconnection scheme adopted by manufacturers and integrators to assure design flexibility. And that, not the 8- and 16-bit sectors, is likely to score the most growth. The Market Information Center, Framingham, Mass., is predicting the 32-bit market will grow more than 150% during the next two years.

But don't count Multibus out yet. The contender should be roaring back within a few years for a rematch. At the same time, a couple of younger challengers, Futurebus and Nubus, could take a shot at the title—admittedly a long-shot for them. And the STD bus and the "no bus" approach—two steady performers that have been in the ring for a while—should hold their own within their own classes.

The rise of VME in this market eclipses the early growth of Multibus. Intel once had the advantage, when it amassed the support of 205 vendors offering 1,325 products for Multibus I, first an 8- and then a 16-bit bus.

Intel launched the first Multibus incarnation as a proprietary signaling scheme to service the Santa Clara, Calif., company's 8088 family of 8-bit integrated circuits. After Intel offered the specification to the Institute of Electrical and Electronics Engineers as a standard for an open bus, Multibus I swept to its dominant position in the market (chart, facing page). Later it was to accommodate the 16-bit 8086.

But as board-level designers started shifting their interest to 32-bit processing, Intel was slow to articulate a migration strategy for those people eager to begin designing a new generation of products. Into this void marched the triumvirate of Motorola, Signetics, and Mostek. In 1981, the three companies jointly offered a specification for an asynchronous 16/32-bit bus to all comers and launched the drive to have it become an approved IEEE standard. VME won an early groundswell of support from those looking for its 32-bit address and data capability. It had a clearly articulated 16- to 32-bit migration path, Eurocard form factors, and pin-in-socket Deutsches Institut für Normung (DIN) connectors (Table 1).

Most important, VME hit the streets nearly three years before Intel announced its 32-bit version of the Multibus, Multibus II. That second incarnation proved to be a radical departure from the original. Multibus I was built around an asynchronous, nonmultiplexed signaling scheme. Multibus II multiplexes address and data on its master parallel system bus using a synchronous communications protocol.

VME—like the Multibus I scheme—is nonmultiplexed and uses asynchronous protocols. VME claims the edge in an asynchronous environment such as process control; however, this same feature complicates the transfer of large blocks of data—a task at which Multibus II excels (Table 2).

There are similarities as well as differences between Multibus II and VMEbus. Both have full 32-bit data paths and address up to 4 gigabytes of memory. Both use DIN connectors in a standard Eurocard form factor. And both have a multiple-bus structure, though the VME uses three pathways while Multibus II uses five to handle data, addresses, messages, input/output ports, and system expansion.

In a Nubus, VME, or Multibus II, reconfiguring a system is as easy as selecting the appropriate I/O boards and adjusting the processing power to accommodate the new requirements. The asynchronous VMEbus is best suited to the interrupt-driven needs of process-control and numerical-control applications in a factory, while Multibus II shines in multiprocessor applications, such as the building of large parallel systems.

When all these relative strengths are tallied, one that appears in the VME column tips the scales—its three-year head start. "The VME world is exploding," notes Fredrick J. Masanec, president of Control Engineering, a San Diego publisher. "We've added 40 new VME vendors in the last six months."

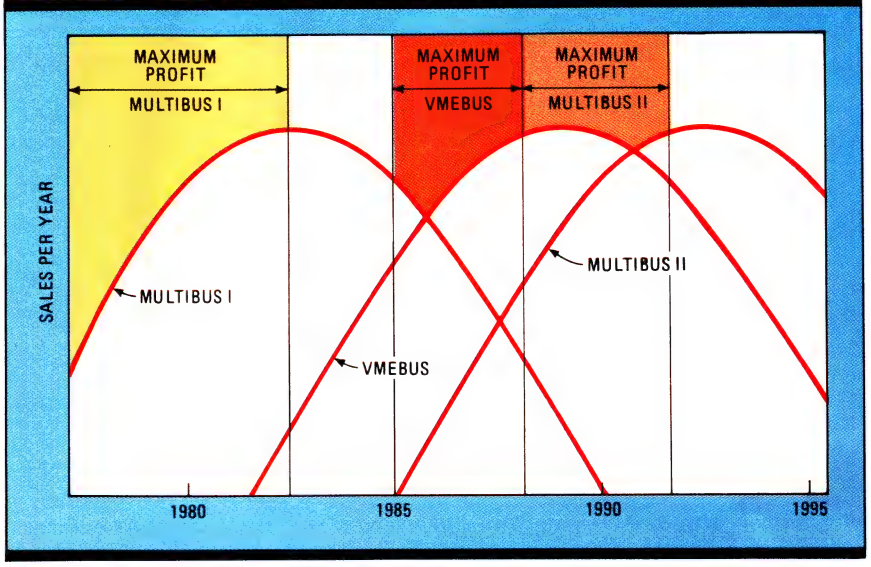
Masanec says the most recent edition of his *VME Buyers*

Guide includes 147 vendors offering 1,051 VME products, whereas Multibus II has won the backing of 21 companies manufacturing 43 boards and other types of equipment. The impressive support for VMEbus brings it close to the backing currently enjoyed by the 16-bit Multibus I, though with one significant difference: "Multibus I is static while VME is still picking up steam," Masanec explains.

In a survey of designers and system integrators, Market Information Center Inc. found both board builders and buyers strongly favoring VME. The market research company asked which bus structure offers the most versatility and long-range usefulness; among the more than 500 respondents, VMEbus held a 3:1 edge over Multibus II. "VMEbus is coming out stronger than we expected," says Harry Henry, president of the Framingham, Mass., company.

Henry sees the migration to 32-bit systems following an orderly growth path, with applications moving from 8- to 16-bit and from 16- to 32-bit systems as prices of microprocessors and support chips drop. His numbers indicate that the next two years should see a drop in demand for 8-bit architectures, a leveling off of demand for 16-bit systems, and a spurt of growth for the 32-bit based architectures.

PRODUCT LIFE CYCLE: VMEBUS THE WINNER IN 1986



16-BIT UNCERTAINTY

In the realm of 16-bit architectures, Henry says, board builders expect to see a 14% net increase in demand—but board buyers expect to see a 6% drop. For Intel's corporate planners trying to predict where the revenue will come from, the big question is whether the 16-bit Multibus I backers will come out in big numbers with Multibus II products.

Intel is gearing up for the selling job needed to convince board manufacturers that Multibus II is worth the investment. Part of the semiconductor manufacturer's strategy is to protect the software investment of the Multibus I customer by providing a link board able to make the asynchronous Multibus I cards run as slaves to the synchronous Multibus II system. The link card resides in the Multibus I card cage and links to the Multibus II card cage. On-board logic handles command translation and address mapping, and translates the hard-wired interrupts of Multibus I to Multibus II's software-defined scheme.

In fact, Intel is playing up the advantages of its software-controlled message-passing coprocessor. The strength of Multibus II message-passing is being touted as the key to building parallel systems. It is also being used to confront VME's strongest suit by claiming superior ability to handle the large number of interrupts generated in an environment such as a factory (Table 3).

Another Intel selling point is the ability of Multibus II to do parity checks on data passed along the bus. The more traditional mainframe manufacturers regard parity checking as akin to an article of faith. Says an engineer for Sperry Corp., St. Paul, Minn., "It's like motherhood and apple pie: sometimes a manufacturer won't even be able to say why they need parity checking, they just know they want it."

Others say adding extra bits for parity checking of data sent across the bus is not worth the trouble. "Seymour Cray was heard to say that parity checking is for farmers," comments John Yarborough, director of the microprocessor-peripherals group of Signetics Corp. The Sunnyvale company is one of the three original VME boosters. Yarborough says a well-designed bus does not require the check.

Whatever the merits of parity checking, Intel's strategy—though belated—is having some success. In addition to Sperry, three other major players—General Electric, Burroughs, and NCR—have jumped on the Multibus II bandwagon.

"Where Multibus has been incredibly successful is in wooing large computer manufacturers off a proprietary bus," says William Clemon, marketing manager of original-equipment-manufacturer systems for Intel Corp. in Hillsboro, Ore. "We won't have the 300 functions for the factory scheme right off the bat, but we'll be able to supply the basics—like central processing unit, disk controller, communications, analog control and data acquisition, and parallel I/O cards—and when the big guys start looking for secondary vendors, I think you'll see support go right through the roof."

Gnostic Concepts Inc., a San Mateo, Calif., market researcher, is predicting Intel will hang on to its dominant market position and be able to shift its customer base from the Multibus I to the Multibus II architecture (Table 4).

"Our take is that Intel will retain its 40%-plus share of the total board market as the shift is made from Multibus I to Multibus II, but they will [have to] fight hard to do it," says Robert Olton, managing analyst. Gnostic pegs last year's worldwide merchant market for board-level computers at $625 million and says it could go to nearly $2 billion by 1988, with $860 million going to Multibus products.

But the word from the trenches is less sanguine. "We have about 600 customers," says Paul Schwartz, president of Qualtech Associates, a Sunnyvale manufacturers' representative. "Eighty percent to 90% of our business used to be Multibus I.

TABLE 1: VENDOR SUPPORT FOR 32-BIT BUSES

	FUTUREBUS	MULTIBUS II	NUBUS	VMEBUS
Developer	Institute of Electrical and Electronics Engineers	Intel	Massachusetts Institute of Technology, Western Digital, Texas Instruments	Motorola, Mostek, Signetics
Backers	National Semiconductor, Ferranti Electronics (possible), Monolithic Memories (possible), Signetics (possible), TI (possible)	21 vendors	TI Lisp Machine	147 vendors
Standardization	IEEE P.896.1, due January 1986	IEEE proposal	IEEE proposal	IEEE P1014

SOURCE: *ELECTRONICS*

TABLE 2: ARCHITECTURE AND PERFORMANCE OF 32-BIT BUSES

Communications architecture	FUTUREBUS	MULTIBUS II	NUBUS	VMEBUS
	asynchronous	synchronous	synchronous	asynchronous
Data paths	multiplexed	multiplexed	multiplexed	nonmultiplexed
Primary (bits)	32	32 at 10 MHz	32 at 10 MHz	16
Secondary (bits)	32, 24, 16, 8	32, 24, 16, 8	32, 16, 8	32, 24, 16, 8
Justification	no	yes	no	yes
Nonaligned transfers	yes	yes	no	yes
Addressability				
Primary bytes	2^{32}	2^{32}	2^{32}	2^{24}
Secondary bytes	expandable	no	no	2^{32}
Broadcast operations	yes	yes	no	no
Data-transfer rate (Mb/s)	117.7	40	37.5 (block transfer)	57 (maximum) 24 (typical)

SOURCE: *ELECTRONICS*

Now all the activity has switched to VME."

Of the 50 to 60 sales leads he gets per day, Schwartz estimates only 1% are inquiries about Multibus II products. "We will rep Multibus II when they are ready, but I think they are still two to three years away," he says.

Others with a long association with the board-level-products market repeat that refrain. When BICC-Vero Electronics Inc., a subsidiary of the English manufacturing company BICC, recently decided to leverage its 20 years in card cage and printed-circuit-board manufacturing production and become a full-service supplier, it decided to back VME. "We owed no allegiance to any processor or bus structure," says Bruce Benysek, a product marketing manager for the Trumbull, Conn., company. "We made our decision based upon the market and the growth potential."

Nubus, which never had firm industry backing, has caught Apple's eye

In several respects, the development of another board-level-product maker parallels the developments in bus architecture. As chief executive officer Bruce Bergman tells it, Xylogics Inc.—the Burlington, Mass., manufacturer of tape and disk controllers—began as a supplier of Digital Equipment Corp. Q-bus products but switched to Multibus I after the latter became an open bus. "We bet the company on Multibus and we won," says Bergman. Now, though, Xylogics is readying a line of VMEbus controllers. "We expect to see VME represent 15% to 20% of our sales next year, though two or three years down the line Multibus II will increase its share."

THE FUTURE BUS

Futurebus and Nubus—two other 32-bit bus architectures—have yet to attract serious industry backing, though the fortunes of Futurebus could pick up early next year and last month Nubus aroused some interest at Apple Computer Corp.

Ever since 1979, the IEEE has sponsored an effort to develop the optimum 32-bit bus. To come up with an architecture that would remain usable into the 1990s, the IEEE's Futurebus group set itself some tough goals: define a standard that is independent of system architectures and microprocessors, optimize it for 32-bit processing, and give it features that will promote interoperability and fault tolerance.

The Futurebus committee opted for multiplexing 32-bit address and data lines using asynchronous protocols. The minimum transfer rate across the bus is 10 megabytes/s, and under simulated conditions the transfer rate has been driven to more than 100 megabytes/s. Two signal lines each are dedicated to address and data-handshaking functions, and a third line permits the slowest module to set the timing during broadcast.

Proponents claim that Futurebus is the first specification to solve the bus-driving problem caused by fully loading a bus with the present generation of TTL transceivers. Current TTL transceivers create noise, and the resulting reflections and crosstalk require enforcement of a line-settling period to maintain signal integrity.

This settling period lowers bus efficiency, so Futurebus backers enlisted National Semiconductor Corp. of Santa Clara to come up with both a 4- and an 8-bit transceiver logic with low capacitance that match Futurebus requirements.

Signetics, Monolithic Memories, Ferranti, and Texas Instruments may announce Futurebus support soon. On the whole, though, the specification has not received overwhelming industry backing. When asked why, the chairman of the IEEE committee says the committee has not actively sought it.

"Futurebus hasn't been officially released, so we are not in a state to encourage implementation by manufacturers," says Paul Borrill, chairman of the Futurebus committee. He will actively discourage interest until the specification is nailed down. Borrill says a publicly released version of Futurebus should be ready for the Buscon '86 show in San Jose in January.

Nubus has never had firm industry backing. It started as a research project at the Massachusetts Institute of Technology, was developed by Western Digital Corp., and finally wound up at Texas Instruments Inc. Apple Computer has demonstrated some interest in Nubus, but it is coy about how serious it is.

An Apple executive says that as part of the company's strategic new orientation toward industry standards, it is looking at all the 32-bit bus structures. "Apple is ready to comment on all the 32-bit buses," says Charles R. Oppenheimer, a hardware product manager, though he concedes that "Nubus is at a point [in the standards process] were they can still take some suggestions."

George White, chairman of the IEEE Nubus standardization committee, says "some people at Apple Computer are seriously considering using the Nubus in a future product." He adds that the committee's last mailing included some proposed changes to the specification suggested by the Cupertino, Calif., company.

The changes are significant. "We're interested in seeing if the committee is willing to adopt a form factor that is compatible with a personal computer and if they are willing to add a single-wire interrupt for low-end personal-computer operations," says David Stewart, an Apple engineer who attended the last Nubus committee meeting.

Like Multibus II, Nubus is synchronous, with multiplexed data and address lines. It supports direct addressability of more than 4 gigabytes of memory through 32-bit addressing and data trans-

TABLE 3: MULTIPROCESSING CAPABILITY OF 32-BIT BUSES

	FUTUREBUS	MULTIBUS II	NUBUS	VMEBUS
Arbitration algorithms	fairness, priority	fairness, priority	fairness	release on request, release when driven
Priority capture	yes (32 levels)	yes (32 levels)	no	yes (four levels)
Deterministic capture	yes	yes, fairness	yes, fairness	yes (four levels) round robin
Message passing	yes	yes	no	no
Virtual interrupts	yes	yes	yes	no

SOURCE: *ELECTRONICS*

actions of 8, 16, and 32 bits. The architecture is completely memory-mapped. It treats all objects on the bus—including memory locations, I/O commands, and interrupts—as locations in memory.

Texas Instruments championed the bus and incorporated it into its Nu Machine artificial-intelligence work station. But TI no longer produces the Nu Machine, though it is licensing the design to Lisp Machine Inc. of Andover, Mass., and is continuing its Nubus efforts through its Explorer AI work station.

Another approach eschews the bus entirely. Many commercial computing applications have few I/O requirements and remain relatively static, so the flexibility and I/O capacities of VME and Multibus II mean little to them. What they need is 32-bit processing with some interfaces for mass storage, back-up, and terminal control. For these applications, a "no-bus" approach can be a cost-effective way to deliver a fully loaded single-board computer.

TABLE 4: WORLDWIDE BOARD-LEVEL-COMPUTERS MARKET

	1983		1988	
	$ millions	%	$ millions	%
MULTIBUS I and II	256	41	860	44
Q-bus	244	38	156	8
VMEbus	50	8	546	28
STDbus	25	4	20	1
S100 bus	19	3	20	1
Other	31	6	351	18
Total	625	100	1,953	100

SOURCE: GNOSTIC CONCEPTS INC., 1985

PUSHING INTEGRATION

Giving the integrator everything needed to build a fully configured 32-bit machine except the power supply and peripherals, Goodspeed Systems Inc., East Haddam, Conn., is building a six-layer, 13-by-15-in., fully loaded single-board computer around the NS32032 (photograph, below). With virtual memory supported by the 32082 memory-management unit, floating-point coprocessing, up to 2 megabytes of dynamic RAM, and a Z80 microprocessor to control a full range of I/O options, the Goodspeed system is part of the trend toward higher levels of integration.

"We're just part of the trend that's pushing application-specific hardware," says Helen Charov, president of Goodspeed. "ASIC on a chip, new graphics ICs, programmable logic arrays, and the 'no bus' concept make it possible to increase functionality while decreasing real-estate requirements."

In the space below the flashy new multiprocessor designs using 32-bit-bus structures, there has been a quiet revolution brewing in 8- and 16-bit buses for the gritty work of factory automation. The 8-bit standard bus, long the workhorse of industrial and control applications, is being beefed up to compete for 16-bit applications.

The STD bus is a favorite for simple control operations because of its small size (4½ in. by 6½ in.), its simple interface requirements, and a plethora of boards for data acquisition and control in industrial applications from more than 150 vendors. Since its introduction in 1978, the bus has kept pace with each generation in processor design, moving from the 8-bit Z80 to the 8/16-bit 8088.

To keep the STD bus up to speed with personal computer technology, its manufacturers are getting ready to interface to the IBM Corp. PC AT bus. For example, the STD Manufacturer's Group at October's Midcon in Chicago gave a warm reception to a presentation by Jerry Winfield, founder of WinSystems Inc., the Arlington, Texas, outfit that specializes in CMOS STD-bus products. Winfield's paper was on multiplexing to handle 16-bit data transfers and full 20-bit addressing while keeping backward compatibility with existing 8-bit I/O cards. His presentation likely will go to the IEEE for inclusion in the specification.

The strategy of the STD-bus manufacturers is to coexist with the PC bus, which is the proprietary bus of the IBM Personal Computer, especially as the IBM PC has taken over as *the* computer on the shop floor.

"The PC provides the access and human interface through its software; the STD bus provides the rugged packaging and a wide operating range using CMOS processors," says Ed Lee, president of Pro-Log Corp., Monterey, Calif. "STD bus is like the arms and legs, the PC is like the eyes and brain."

While the STD bus is pushing upward, the PC bus is making a bid in markets presently served by Multibus I. "The AT bus is encroaching on Multibus I and low-end VME applications," says Nick Antonopoulos, product marketing manager for Faraday Electronics, a Sunnyvale company that started out in 1983 as a single-board-clone business and projects $24 million in sales for next year. Faraday is supplying a full line of PC-bus products, including a 3-by-5-in. single-board computer with a custom CMOS processor said to replace up to 34 low-power Schottky chips and the entire Intel chip set except for the 8088.

"The PC has become the engineering work station of choice; it has shaken up the engineering community," notes Robert A. Burckle, vice president of WinSystems. □

NO BUS. With the trend toward greater levels of integration on a single board, Goodspeed Systems offers fully 32-bit computing on a single board.

ADVERTISEMENT

Intelligent I/O Channel for VMEbus...

PEP Modular Computers has taken a quantum technological step forward with its Intelligent I/O Channel/Eurobus. It is currently the only bus system on the market which allows use of the most common 8-bit (internal 16/32-bit) microprocessors in NMOS or high-speed CMOS, with the added flexibility of combining these traditional and future-oriented technologies.

Despite its design sophistication, the IIOC/Eurobus is extremely easy to use and offers low-cost interface requirements. With 20 address lines and 8 bi-directional data lines, the IIOC/Eurobus supports all the major low-cost microprocessors in HCMOS and NMOS—including the 68008, 8088, 68HC09, 68HC11, Z80, and others—for industrial applications with a minimum of power consumption at a maximum of reliability.

It offers standardized single-sized Eurocards (100 x 160mm) with 64-pin indirect DIN connector, and can be used in harsh environments and military applications.

The synchronous access to I/O and memory with a bandwidth of up to 3 Mbytes/s supports master and slave modules, independent of their physical position on the bus. This is possible because all addresses are fully decoded and the I/O is memory mapped. Optional asynchronous access supports especially high-end 8-bit microprocessors like the 68008 from Motorola. It is also possible to access 64-Kbyte synchronous memory-mapped I/O.

VME systems with low-cost I/O. PEP and other second-source suppliers offer a broad range of low-cost I/O modules for the IIOC, in most cases eliminating high development costs. Development resources can be assigned for dedicated HW- and SW- projects.

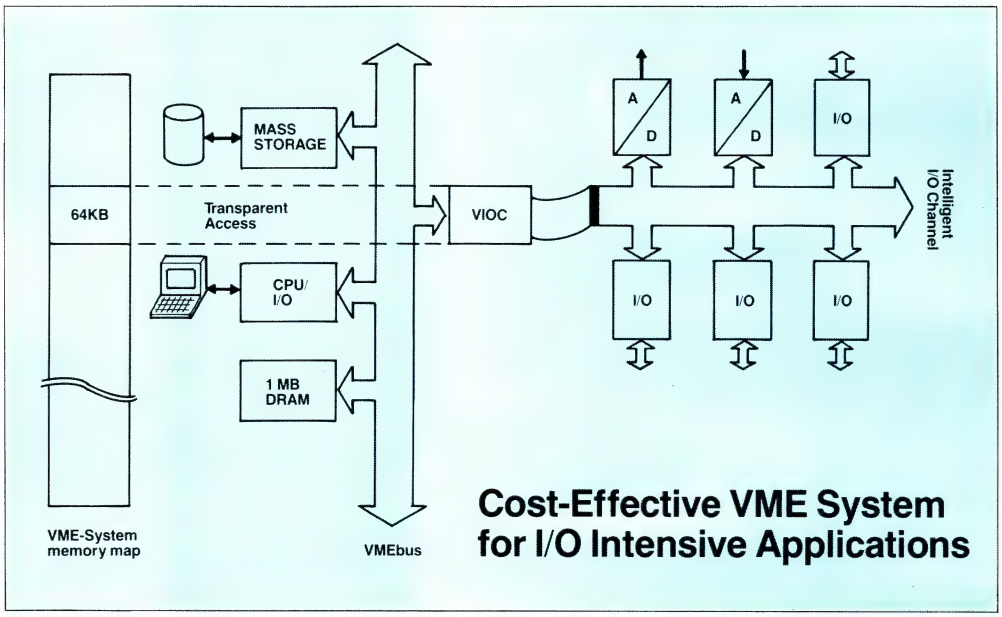
In data acquisition systems or graphic applications, it often is desirable to accomplish some data preprocessing with an 8/16-bit CPU—such as a 68008, 6809, Z80, or 18085—locally in the I/O channel before data is taken over by the master CPU on the VMEbus. The I/O operations and the preprocessing thereby are not occupying the VMEbus. This increases system throughput.

Depending on the application, the CPU on the IIOC may either run an application program in ROMs, or run under a ROM-OS, or a disk operating system such as CP/M, Flex, or OS-9, while the VME system runs under OS-9/68K, VERSAdos or another OS.

I/O channel in single height. Solutions for I/O intensive applications realized on the VMEbus only are quite expensive because of the costly I/O cards. The design of cards for the asynchronous VMEbus with its complex timing requires more time and cost than comparable I/O cards on an 8-bit synchronous I/O channel. I/O operations are usually slow and would reduce the throughput on the VMEbus. Having an I/O channel which allows direct portability with transparent access from the VMEbus eliminates those disadvantages. Because it uses modules in single height Eurocards, complete systems consisting of a VMEbus and IIOC can be built up in a common single height format.

But the IIOC from PEP is more than just an I/O channel. The architecture is based on the Eurobus and allows a local I/O processor. The heart of the PEP concept is a VMEbus-to-IIOC communications controller (VIOC). This is a single-height module which occupies one physical slot (P1) and 64 kilobytes of addressing space anywhere on the VMEbus. It is possible to have more than one VIOC installed in a VME system. Existing VME systems with double height modules may also be expanded with the VIOC. The board size and connector are standard single-height Eurocard (3.95 x 6.3 in.) and an IEC 603-2 Connector (64 pin).

The VIOC module has a flat cable of up to 50 cm in length which connects directly to the backplane of the intelligent I/O channel. The VIOC module contains all synchronization logic to allow a CPU on the VMEbus a transparent access to each memory location or peripheral register on the IIOC in a byte- or word-mode. The access time is around 2 microseconds, depending on the type of access, byte or word. If a word has to be read from the IIOC, the first byte is stored in an on-board register for the VIOC and transmitted together with the second byte as one word on the VMEbus. This concept allows the use of a broad range of low-cost I/O modules on the IIOC in a way as if they would be on the VMEbus, but eliminating the complex bus interface on each card.



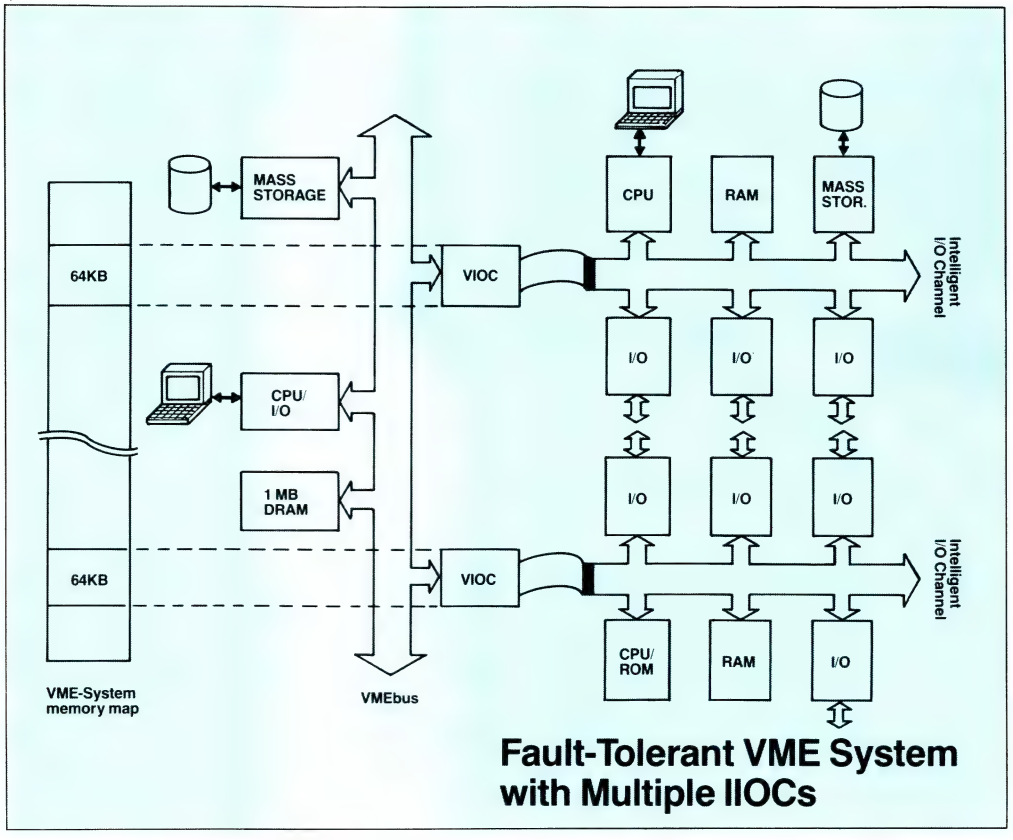
Both CPUs run simultaneously at full speed only if the CPU on the VMEbus wants to access the IIOC, the VIOC module automatically requests a DMA on the IIOC for each transfer. If there is another DMA controller on the IIOC (i.e., a floppy disk controller) it has higher priority than the VIOC. It is important to know that the master CPU on the VMEbus has access to the IIOC; however, the slave CPU on the I/O channel has no access to the VMEbus. Communications between the CPUs can be implemented by using interrupts or flags indicating a ready condition. Messages and data can be exchanged via a common memory area on the IIOC which is used as a mailbox without the need of dual-ported RAM. Powerful multi- and co-processor systems are possible without the need of complex communications software.

VME system with more than one IIOC. As mentioned above, it is also possible to have more than one IIOC connected to a VMEbus. There is only a physical limitation due to the maximum length of the flat cable between the VIOC module on the VMEbus and the IIOC backpanel. It is also possible to run different operating systems on different I/O channels.

. . . supports NMOS and HCMOS microprocessors

Communications between the various I/O channels works then through the master CPU on the VMEbus. Power supply produces +5V and +12V, with +5V standby.

The PEP concept is a cost-effective way of implementing complete VMEbus systems including an I/O channel for applications which require lots of I/O or powerful multi- and co-processing capabilities, all in a compact single Eurocard. Supported by a worldwide network of vendors, which guarantees service and product availability, the Intelligent I/O channel/Eurobus is the standard bus architecture for future oriented industrial designs with a direct link to the industry standard bus for 16/32 bit, the VMEbus.



Fault-Tolerant VME System with Multiple IIOCs

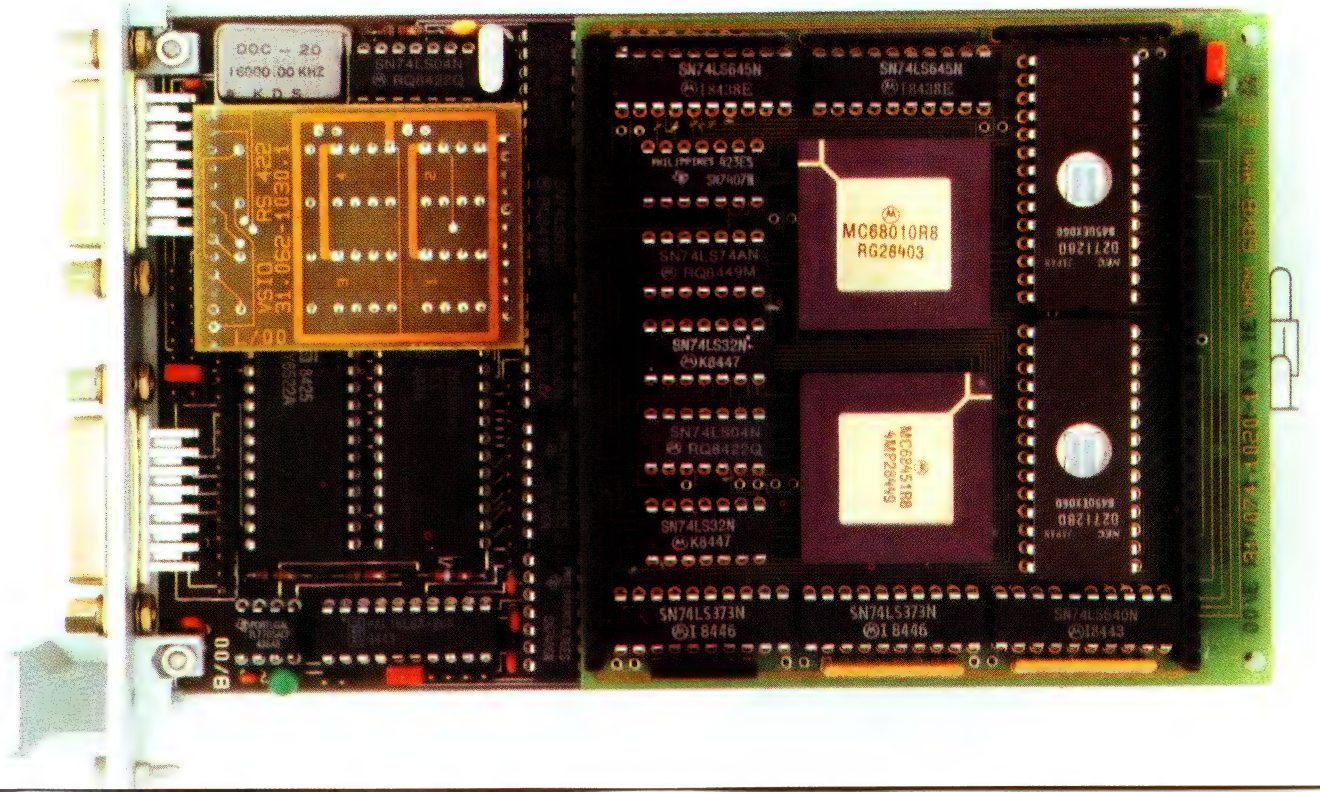
Get your free bus specification from

Modular Computers®

US: PEP Modular Computers, Inc., 600 North Bell Avenue, Pittsburgh, PA 15106
Phone: (412) 279-6661, Tollfree: 1-800-228-1737 (outside PA), 1-800-255-1737 (inside PA)
Telex 6711521, Telefax 412-279-6860

Europe: PEP Electronik Systeme GmbH, Am Klosterwald 4, D-8950 Kaufbeuren
Phone: (08341) 8974, Telex 541233, Telefax (08341) 40422

Circle 53 on reader service card



©1985 AT&T Information Systems. IBM is a registered trademark of International Business Machine Corp.

HOTLI

AT&T'S SMALL BUSINESS CONNECTION.

Take your pick from our family tree.

Whether you're looking for the ideal telephone system, computer, or FAX machine for your small business, there's a connection.

They're all members of AT&T's Small Business Connection—a full family of products and services specifically created to help you save time, effort and money.

It's easy to connect with the Small Business Connection. Simply dial 1 800 247-7000, our hotline, and you'll immediately be in touch with a specialist trained to understand the needs of small businesses. A specialist who'll work with you to tailor an equipment and service package that fits your individual needs perfectly.

While you're on the line, you'll learn about AT&T's hot line of products. Like the MERLIN™ Communications System,with features like conference calling, which lets you conduct time-saving meetings over the phone. Or speed dialing, which instantly puts you in touch with key people. Features you can program and reprogram to meet your changing needs.

When it comes to surefire products, there's nothing like our full line of computers, including AT&T's 3B Computers and our new popular AT&T UNIX™ PC The UNIX PC delivers the kind of power, speed and exceptional ease of use few PCs can match. Not to mention AT&T's PC 6300. It's fully compatible with the IBM PC yet twice as fast

Get the total telephone for small business.

NEC

AT&T GIVES YOU ONE NUMBER TO REMEMBER FOR UNFORGETTABLE PRODUCTS AND SERVICE.

1 800 247-7000
EXT. 204

This number connects you to the office in your area.

and more expandable.

You'll also get all the facts on the AT&T FAX 3510D. It's capable of firing sharp, clear copies of letters, charts or photos—across town or across the country—as fast as 20 seconds a page. Plus it's industry compatible, fully portable, and completely automatic.

Send stacks of tracts in a flash with this FAX.

Finally, we'll wrap it all up for you in one of our service packages, like Service-Plus. This allows you to take care of all your communication needs with one call. You can even select one of several financial plans to meet your cash flow requirements.

Best of all, along with everything else comes all the experience, resources and know-how only AT&T can offer.

Use the hotline and call AT&T's Small Business Connection today. Just dial 1 800 247-7000, Ext. 204.

You'll be warmly received.

SERVICE PLUS

Service-Plus is just one of the plusses.

AT&T

The right choice.

Circle 55 on reader service card

EXPERT SYSTEMS TACKLE VLSI TESTING

AI PROMISES A THREE-LANE HIGHWAY OUT OF THE TEST SNARL

by Jerry Lyman

Artificial intelligence is starting to make its presence felt in the world of automatic test equipment—and not a moment too soon. Chip and system makers are finding that their integrated circuits and the boards onto which they are packed are becoming too complex to be tested by existing equipment.

Test equipment based on the principles of AI promises to give harried users a three-lane highway out of the testing snarl. AI, and expert systems in particular, is well on its way to becoming a standard feature of ATE from the major manufacturers in the field.

The technology punches up testing in three ways. First, it incorporates the knowledge of many experts. The user can also build up the knowledge base as he learns more about the test process. Second, ATE is better equipped to sniff out trouble spots. Up to now, "software has been used to aid in detecting faults," says A. Jesse Wilkinson, software engineer at Teradyne Inc.'s Woodland Hills, Calif., facility and a recognized authority in the field. "[But] this software reported symptoms—it did not give any indication as to the source of the fault." With AI, it can.

Third, AI as a diagnostic tool of ATE radically cuts downtime. With test systems selling for $2.5 million or more, idle time is extremely costly.

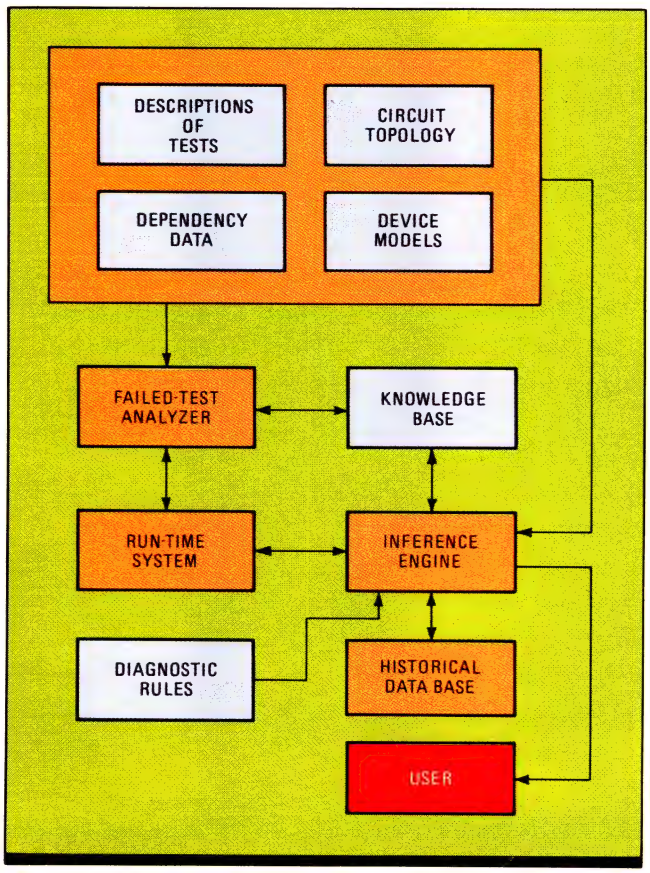
It should come as no surprise that the International Test Conference in Philadelphia last week was the scene of a good deal of talk about AI. Five papers on the topic were presented—two more than in 1984.

Teradyne put in the strongest showing with three papers. One, from its Boston operation, discussed an expert system for in-circuit fault analysis. The others, from Woodland Hills, covered an expert system for diagnosing system faults in the J941 very large-scale-integration logic tester. There was also a paper from GenRad Inc.'s Design Engineering Group, Santa Clara, Calif., describing an expert system to check the testability of digital IC designs, and one from Texas Instruments Inc. presenting a rule-based approach to classifying switch-level faults in CMOS circuits.

"With so many nodes active during a VLSI in-circuit test, conventional in-circuit diagnostics that were fine with [small- and medium-scale integration] boards have become much less effective in isolating faults," noted Teradyne's Larry Apfelbaum in his paper on in-circuit testing. He pointed out that each true fault that occurs on a board can generate several apparent faults because the faulty node or device might be part of an isolation strategy for other devices on the board. If these other devices are not isolated during in-circuit tests, they might appear to fail when they are in fact good. Conventional in-circuit diagnostic algorithms do little to aid in the detection of such shortcomings.

REPLACING THE TECHNICIAN

The paper described how expert-system software replaces a skilled technician in analyzing the test-failure data by deciding if additional measurements are required (Fig. 1). If so, the software creates a simple repair message by using a rule-based system. The Teradyne system is based on the software language Bliss rather than on Lisp, the standard AI language. "We are in a production environment and time is money," Apfelbaum said. "Most AI languages are fine, but they take up a lot of memory space and need a lot of time to operate."



1. IN-CIRCUIT EXPERT. Expert software replaces a skilled technician by analyzing in-circuit test-failure data and creating a repair message.

The diagnostic system has three major components: a coordinated test-generation facility, a failed-test analyzer, and a diagnostic inference engine. The first component's task is to evaluate an appropriate, effective in-circuit test for each device during in-circuit test generation. The test generator, sometimes called a composer, must also understand the constraints imposed by circuit topology. It must then merge any user test requirements and write the actual test.

Access to all the information that the composer used during test generation is a key element of the diagnostic process. This information is saved in a knowledge base containing information about all boards of the type under test, including which tests are appropriate, the circuit nodes involved directly in each test, and how they relate to the test.

The failed-test analyzer intercepts all failures reported

by the tester's run-time system during testing, and analyzes them as they occur. When a test fails, the analyzer interrogates the circuit knowledge base to determine if further analysis is needed. If so, the analyzer can ask the run-time system to interrogate other nodes involved in the test.

In this manner, the failed-test analyzer acquires additional data about the test to build a more robust description of a failure. It then adds that information to a knowledge base that contains information unique to the particular board test.

Once testing and failed-test analysis have been completed for all devices, the diagnostic process can begin. The knowledge base has been filled with all of the test results for the board. Data bases from the composer are also available to the inference engine—the mechanism for interpreting expert knowledge and controlling the diagnostic process.

Diagnostic rules reduce irrelevant and erroneous failure data

The diagnostic process has several phases. In each, the goal is set—which fault category or symptom is to be examined—as is the domain in the knowledge base that is relevant to the failure. The knowledge bases for each board have domains for three major types of failures: digital device, analog device, and nodal. The domains are linked so that the program can evaluate relationships between failures.

Associated with each domain is a set of diagnostic rules, which operate in an environment that is optimized for the class of failure being diagnosed. For example, functional failures are device-oriented, whereas bus failures are nodal in nature.

The objective of the rules is to reduce large amounts of failure data to small amounts by filtering out erroneous or irrelevant results early. When faults have been identified, the knowledge base is modified so that the new data can be used to evaluate the remaining faults.

OF A SIMILAR MIND

Teradyne also has put together a system that repairs ATE. Designed to embody in software the knowledge of many test-system repair experts, the system is called MIND, for Machine for Intelligent Diagnosis (Fig. 2). For the past year and a half, Teradyne's engineers and software experts have been developing the first version of MIND for the J941 VLSI logic tester with the aim of reducing the mean time to repair of this large-scale test system. MIND uses the Teradyne M963 (the J941's main processor) as its inference engine.

MIND is constructed in the working language of the test system—Pascal or C, in the case of the J941. The use of the native tester language has several advantages over an AI language such as Lisp, according to Wilkinson, coauthor of the two papers on the system. First, MIND's problem-solving capability is not so much in the processing of the knowledge as it is in the actual quality of the knowledge itself. This repair knowledge is not a function of the language chosen for implementation. Second, the native language affords a much greater control of the hardware under test.

During the process of rule evaluation, the inference engine interacts with subparts of the MIND system. For example, it gets its primary input from the diagnostic data base. While evaluating these rules, the conditions to be evaluated and the actions to be executed are carried out by the inference engine.

Teradyne plans to test a J941 with MIND at a beta site in the first half of 1986. The system will be an option on the J941 and future Teradyne VLSI testers. When MIND does reach the field, the company will continuously update its knowledge base.

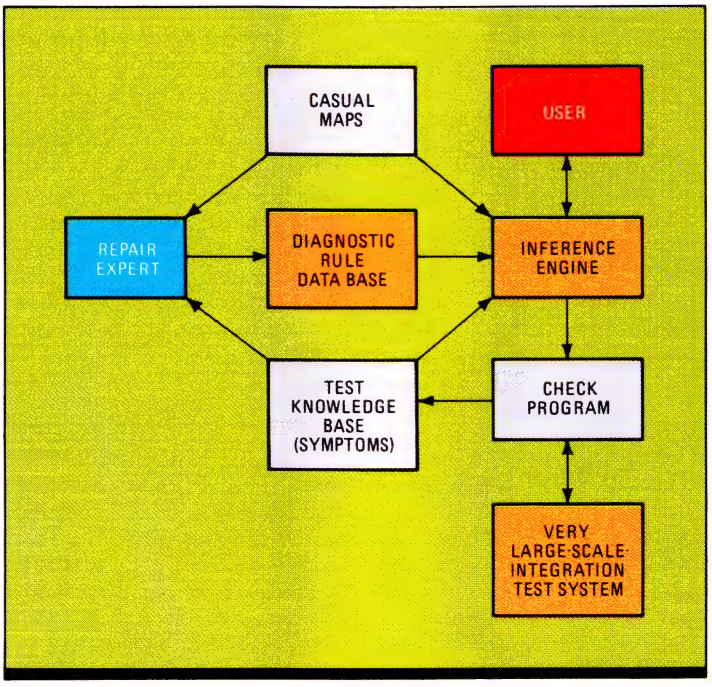
The computer-aided-design system described by GenRad is one answer for the VLSI designer who is not an expert on test technology but wants to make certain that the circuit he is developing is testable. A paper by Kyushik Son of GenRad's Santa Clara Design Engineering Group talked about a system under development that generates tests and rules to measure testability of a digital IC's design. Design rules for off-line testability methods are specified either topologically or semantically in a knowledge-base system. The purpose of test generation, using testability design rules, is to maximize the availability of extra circuitry for testability.

This system concentrates on off-line testability techniques commonly called scan designs, a scheme for obtaining perfectly controllable and observable sequential devices through a scan path. This can be done in a serial, parallel, or random fashion. One popular serial-scan method is IBM Corp.'s Level Sensitive Scan Design (LSSD), in which shift registers are chained together to form a giant scan path.

The proposed system for testability analysis and test generation evaluates a design against design rules for testability, edits the region-violating testability criteria, and then generates a set of test patterns for the constrained design. There are three major components: testability checker, circuit editor, and test generator.

Design rules for a testability method are specified in the design-rule knowledge base. Generic signals and topological data are loaded into the circuit data structure. Semantic checking is done using a simulator running Hitest, which is software for an expert system for test generation that was developed by Cirrus Computers Ltd. in England, with waveforms from the knowledge-base system. Finally, the combinational test generator of Hitest will be used to generate test patterns by using the design-rule base.

The final system, from TI, is the only one at the conference that uses the more conventional AI languages, Lisp and Prolog. It deals with a classification of faults in CMOS circuits based on the behavior of the faults during simulation. The approach is rule-based; the classification system, implemented in Lisp and Prolog, is used to spot and eliminate the faults—20% to 40% of them—not detectable before simulation. □



2. TEST-SYSTEM DIAGNOSIS. MIND, the Machine for Intelligent Diagnosis, reduces the mean time to repair of large test systems.

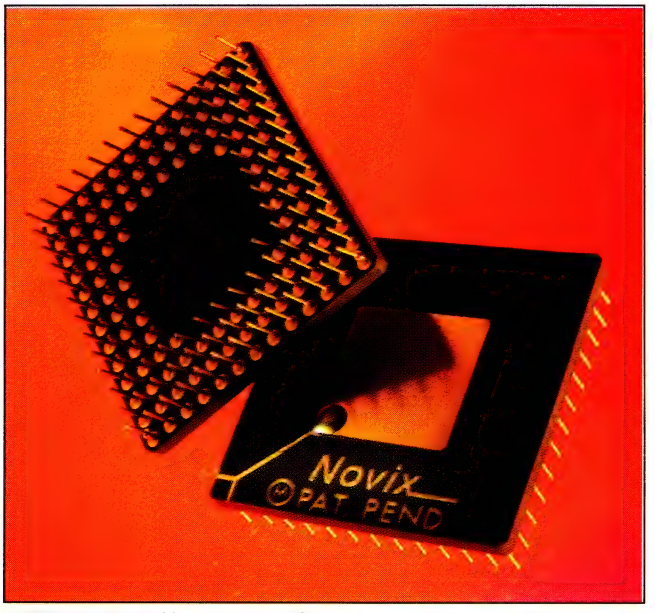
A PRIDE OF NEW CPUs RUNS HIGH-LEVEL LANGUAGES

'LISP-ON-A-CHIP' COULD ACCELERATE USE OF AI IN SMALL COMPUTERS

by Bernard Conrad Cole

About to emerge from the labs are the first high-level-language processors, some as single chips and some as computers on a board. Such "Lisp-on-a-chip" or "Forth-on-a-board" central processing units operate as coprocessors with more general-purpose CPUs and could accelerate the development of small computers based on languages used to write artificial-intelligence programs.

Many in the industry believe that systems built around AI-based high-level-language-specific processors could make personal and small business computers considerably easier to use. This would open up the market to a broad range of unsophisticated users, says John L. Hennessy, director of Stanford University's Computer Systems Laboratory in Palo Alto. Expert-system application programs also could get a boost.



FORTH ENGINE. Novix's 16-bit CPU Forth chip has 4,000 gates.

Until recently, most efforts at developing language-specific CPUs were confined to academia, such as the Massachusetts Institute of Technology's Scheme chips, built around a variant of Lisp and the SOAR (Smalltalk on a RISC) processor from the University of California at Berkeley. But with the availability of advanced bipolar and CMOS very large-scale integration technology, high-level-language-specific processors are emerging from the university laboratories and toward commercial realization.

At the just-ended Wescon in San Francisco, for example, initial efforts in this direction were described by representatives of eight companies. These ranged from large multimillion-dollar concerns aiming for applications in the military to entrepreneurial startups formed by programmers and designers who are frustrated with the high cost and low speed of systems currently used to develop AI-based expert-system and robotic-application programs for industry.

Eight companies have language-specific chip or board CPUs

Although it is generally agreed that support of high-level languages is an important aspect of microprocessor design, most implementations do not go as far as many users would like. On the CISC side, most recent 32-bit microprocessors, such as National's 32332, Intel's 80386, and Motorola's 68020, claim to provide such support by implementing data structures and machine-level instructions that simplify programming using high-level-language compilers and interpreters.

But there is a tradeoff for this increased complexity: some reduction in throughput. Some makers of CISC CPUs try to compensate for it through process improvements and architectural enhancements such as pipelining and on-chip cache and memory management. Other companies, such as Harris, Hewlett-Packard, Inmos, and MIPS Computer Systems, have opted for the RISC approach, which IBM Corp. pioneered with its 801 processor. In this method, high-level languages are supported the same way as with CISC computers but with fewer instructions. The CPU's instruction set is streamlined and optimized for a particular application environment, resulting in significant improvements in throughput.

But high-level languages cannot be executed directly with either approach, according to David C. Wyland, senior research engineer at SRI International in Menlo Park, Calif. This means that such languages must be transformed to the machine level. At present, not only are high-level languages available only in compiled or interpreted form on conventional architectures but they carry substantial performance penalties. For example, conventional architectures require inordinate memory traffic to accomplish even such simple operations as loading registers, says David Winkel, a designer at Logic Design Inc., Bloomington, Ind. "Useful [high-level-language] constructs must in turn be synthesized from these primitive machine operations."

Such penalties increase with the sophistication of the language as it moves further along in the high-level evolution. The problem is acute in the more advanced problem-oriented "nonprocedural" languages such as Smalltalk, Forth, Prolog, Lisp, and Ada. Because they are more English-like in their construction and syntax, they execute more slowly than older procedure-oriented languages such as Basic, Fortran, Algol, and Pascal.

The problem, says Wyland, is that it is precisely these nonprocedural languages that are receiving the most interest in academia, industry, and the military in such areas as automatic program generation, system simulation, natural-language translation, intelligent data-base systems, and AI-based robotics and knowledge-base applications.

The high-level-language processors discussed at Wescon

take dead aim at this problem. Rockwell International Corp. has chosen Ada for its target implementation. Texas Instruments Inc. is developing, under contract to the Defense Advanced Research Projects Agency, a Lisp-on-a-chip implementation of its current board-level product, the Explorer. Four of the companies—Hartronix, Logic Design, Novix, and Radionics—have developed processor architectures optimized for Forth. Xenologic has focused its efforts on Prolog. Finally, there is Tantivity Associates, which has developed an architecture that allows implementation of any one of a number of nonprocedural languages onto a semicustom array.

AIMING FOR THE SKY

The most mature of the chip-design efforts is that of Rockwell International's Collins Government Avionics Division in Cedar Rapids, Iowa, which is in the preliminary stages of its third design effort aimed at military avionics. Now in production is the single-chip 16-bit Advanced Architecture Micro Processor, or AAMP. Designed to efficiently support the execution of block-structured high-level languages such as Ada, Jovial, and PL/1, the AAMP instruction set includes multiplication and division for 16- and 32-bit integer and fractional data as well as 32- and 48-bit floating-point data.

Rockwell implemented the instruction set in two processes: CMOS-silicon on sapphire and bulk CMOS. Now available is the SOS version using 2-μm geometries and polysilicide interconnections. Operating at 20- to 30-MHz clock rates, a typical die measures 241 by 264 mils and has a power dissipation of about 55 mW. Measured by the industry-standard Whetstone benchmark, the SOS version has a throughput of 285,714 Whetstones per second using a 30-MHz clock. Scheduled for first silicon by the end of this year, the bulk-CMOS version uses double-level metal interconnection and 2-μm design rules with n-type wells, substrate, and well contacts. Measuring 243 by 262 mils, it operates at 20 MHz and dissipates 200 mW.

In the preliminary stages of development is an extension of the AAMP architecture called the Ada-directed Collins Adaptive Processing System (Acaps), according to Jeffrey D. Russell, one of the designers. As with AAMP, the Acaps architecture uses a process stack for local environment, procedure linkage, and accumulator stack operations. A single-chip implementation in 1.25-μm bulk CMOS is planned that will use full 32-bit data paths and a 32-bit linear addressing space. Projected throughput will approach 1 million Whetstones/s, about equivalent to that of a Digital Equipment Corp. VAX-11/780.

The Acaps was designed initially for direct execution of Ada, says Russell, but there is nothing about the architecture of any of the parts that rules out its use in silicon to implement any one of a number of other high-level languages such as Forth, Prolog, or Lisp. In fact, investigations are under way at the Collins division in Cedar Rapids to convert the architecture to Lisp.

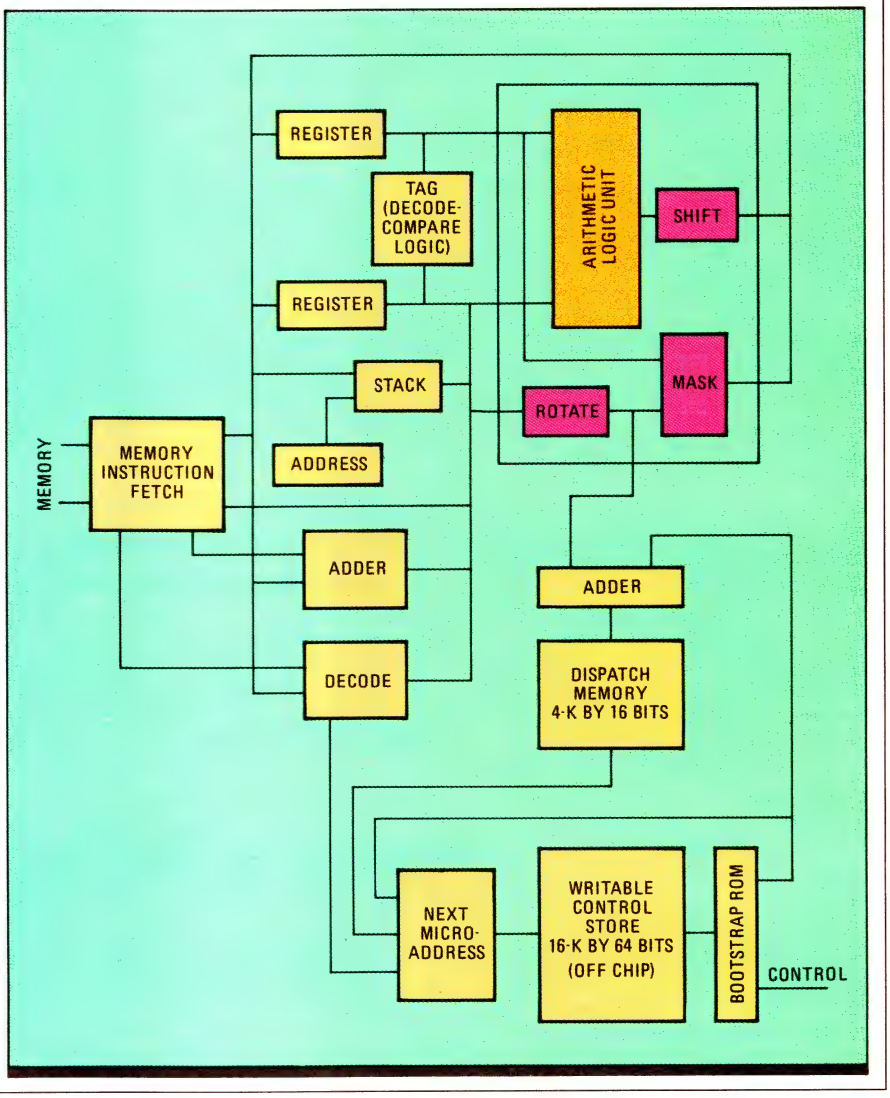
Further along in its Lisp efforts is Texas Instruments, Dallas, with its Compact Lisp Machine (CLM), a 32-bit processor microprogrammed to support Common Lisp (figure, below). Fabricated in sub-2-μm CMOS, the CLM processor is in the final stages of design. TI expects it to operate at a clock frequency of 40 MHz and hopes to have first-pass samples available near the end of the year. Although developed under contract to Darpa, the 32-bit Lisp chip might be used as a coprocessor in TI's Professional Computer series, which is compatible with the IBM Personal Computer. It could be the machine that opens up the personal computer marketplace to a wider range of users who have been intimidated by present systems.

The CLM contains two main functional units—the arithmetic logic unit and the shifter and masker. The ALU is of conventional design with additional provisions for performing arithmetic and logical operations on typed data, although it can be used for untyped operations also. The shifter and masker support bit-field operations and can rotate up to 32 positions.

Of the Forth processors, the most ambitious and furthest along in development is the implementation from Novix Corp., Cupertino, Calif. [*Electronics,* Aug. 19, 1985, p. 41]. Introduced earlier this year, the NC4000P is a special-purpose 16-bit CPU fabricated on a 4,000-gate semicustom array using 2-μm double-level metal CMOS processing. Designed for direct execution of Forth, it can operate at an 8-MHz clock rate with a throughput of 10 million operations per second.

On a less ambitious level, several implementations of Forth on a board are in various stages of development or produc-

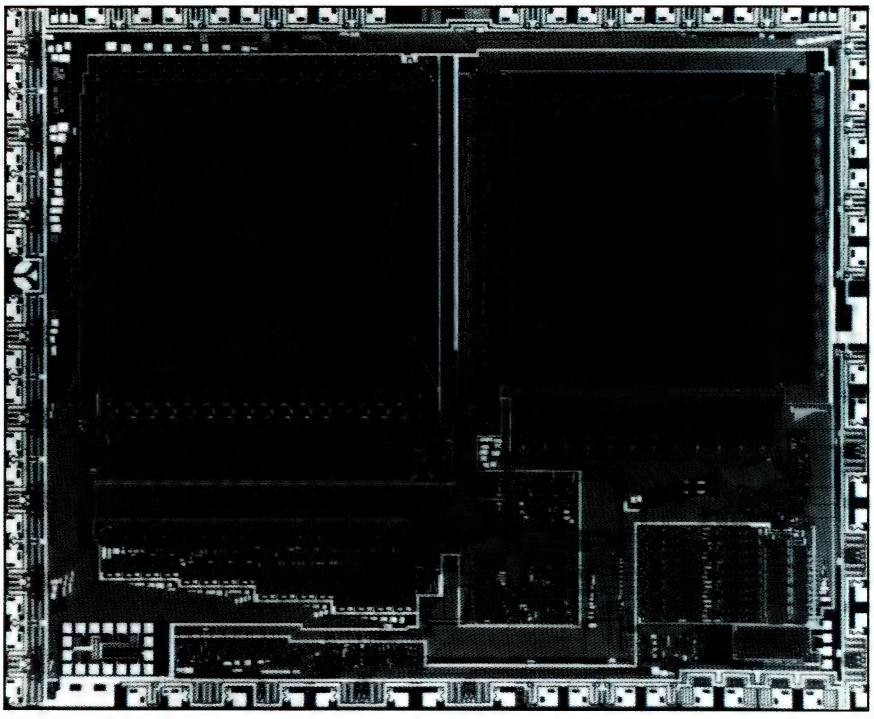
LISP CHIP. TI's Common Lisp Machine has two units: an ALU and a shifter and masker.



tion. For example, Logic Design is currently in the breadboard-prototype stage with its Forth machine, a 164-chip design that incorporates the 2910 microsequencer and the LS181 ALU. The company plans to implement the data-path structure with programmable-logic-array (PLA) circuits, which will reduce the machine's chip count to 68.

Two single-board Forth processors are also in the battle. From Hartronix Inc. of Tempe, Ariz. comes a 16-bit processor using off-the-shelf bipolar bit-slice circuits. And Radionix Inc. of Salinas, Calif., has a model that exploits the capabilities of three still-to-be-introduced bipolar large-scale-integration building blocks from Monolithic Memories Inc., Santa Clara, Calif.

Linked by a network of PALs, the key elements in the Radionix design include Monolithic Memories' 57/677082 16-bit ALU, featuring three working registers, three levels of on-board carry/look-ahead logic, and a 16-bit output register that can be bypassed using flowthrough logic; the 57/677530, a 32-by-32-bit shift-matrix circuit that can be cascaded to long word lengths with just one level of logic delay; and the 74S556 Cray multiplier, which differs from other implementations in that all 32 bits of an entire double-length product are available simultaneously at the outputs instead of being multiplexed out in two 16-bit groups over input/output pins.



TWO FLAVORS. Rockwell's AAMP chip supports Ada, Jovial, or PL/1 in CMOS or CMOS-SOS.

PROLOG USING STANDARD PARTS

Taking a somewhat cautious route—it builds its processor out of standard bit-slice components—is Xenologic Inc., Berkeley, Calif., with its two-board Prolog-based X-1 coprocessor designed for use on VMEbus systems, allowing it to be embedded in a variety of computer systems. Intended for operation as a slave processor, it can perform between 200,000 and 300,000 logical inferences per second (lips), a number that is roughly equivalent to operation on an IBM 3081 mainframe. By comparison, says designer and company cofounder Alvin Despain, a Z80-based personal computer running the same logical sequences using MicroProlog can perform at only 120 lips. Comparable operations performed on a VAX-11/780, depending on implementation, range in speed between 1,500 and 15,000 lips.

Still needed: low-cost, high-speed development systems

The most flexible high-level-language-specific design is a structured language computer (SLC) under development at Tantivity Associates, Palo Alto. The SLC has an architecture that can be configured for use with a number of high-level nonprocedural languages. Although initial designs are built around Forth, its designers, James Vaughan and Robert Smith, believe that the same basic architecture can build a Pascal, Ada, C, or Lisp computer that is based on the same principles.

In this architecture, the SLC is split into two independent hardware pieces: the computational element and the sequencer. Communications between the two elements is through a program memory bus. The computational element is a coprocessor that performs all of the traditional arithmetic operations. Getting its instructions and data from the sequencer, the computational element is similar to TI's 74181 ALU. The key to the design is the sequencer, which takes advantage of the fact that most high-level languages resemble a tree structure. Implementing a standard architecture for traversing a tree, it performs the sequential operations, such as Call, Return, Branch, and Continue. In most cases only six instructions are needed to generate a working instruction set.

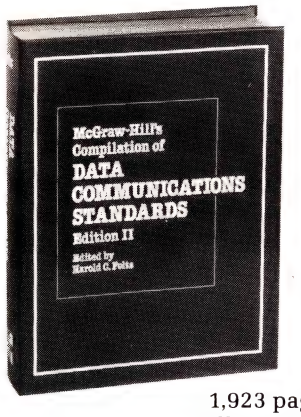
In its current breadboard form using off-the-shelf bipolar components, the Forth implementation of the architecture runs at a speed of about 10 million instructions per second, running most of the standard Forth words. This is about 10 to 40 times the throughput that can be accomplished with a conventional superminicomputer, says Vaughan. Simulations of the basic architecture, he says, indicate that it can be implemented on a 6,000-gate CMOS semicustom array using processing independent of language and with little or no loss in throughput.

The most immediate and dramatic impact of such single-board and single-chip language-specific designs, according to Stanford's Hennessey, will be in the development of low-cost, high-speed development systems. "Currently, the only options available to a programmer working in one of these languages—if he wants a reasonable turnaround time—is to work on a conventional mainframe or on one of the specialized minicomputer-based development systems. That is an alternative that is available only to a large company. With the emergence of board- and chip-level [high-level language]-specific designs, program-development systems will eventually emerge that are within the range of the individual programmer and systems designer, increasing dramatically the development of application programs using languages such as Lisp, Prolog, and Forth."

Initial demand for such processors, says SRI's Wyland, will come from the military and industry for applications requiring real-time execution, such as robotics and pattern recognition. Ultimately, says Novix general manager John Golden, as more and more such designs become available in chip form, they will be incorporated into a broader range of computing systems, operating as coprocessors with CPUs of conventional design, where they will be called into action when the application requires it. □

NEW EDITION

All standards are new, revised, or reaffirmed since the previous edition



1,923 pages
illustrated
Edited by Harold C. Folts

DATA COMMUNICATIONS STANDARDS

All 123 interface protocol standards set by:
• CCITT • ISO • ECMA
• ANSI • EIA
• U.S. Government

Special feature for instant access to the applicable standards:
Cross-reference tables of the similar and interfacing standards of each standards organization.

Electronics Magazine Books
P.O. Box 541
Hightstown, NJ 08520
609/426-5070

Please send _____ copies of R100-*McGraw-Hill's Compilation of Data Communications Standards Edition II* at $295 each.

Name

Title

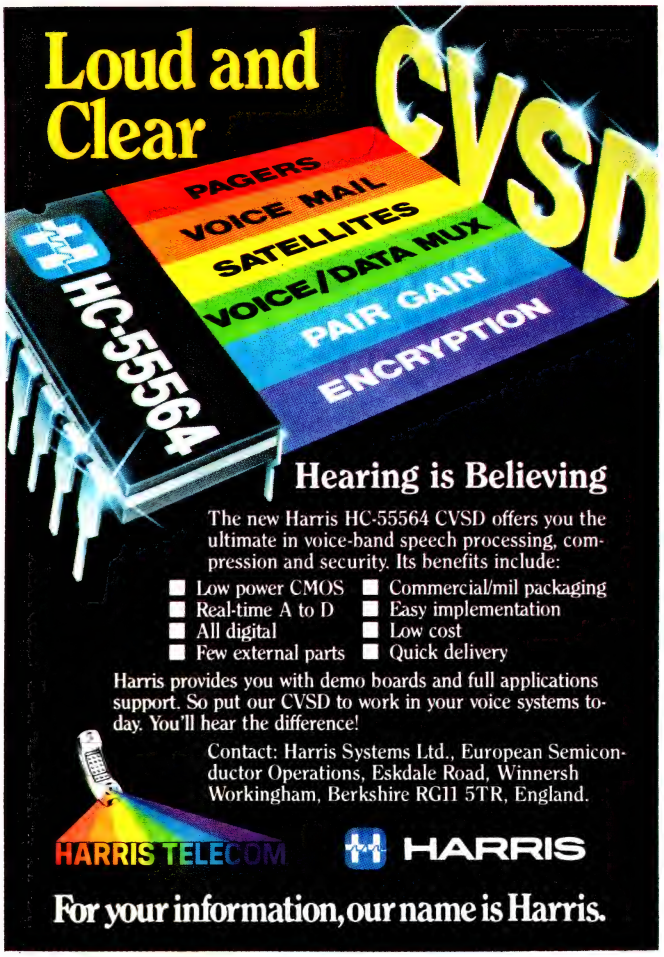
Company

Address

City/state/zip

U.S. customers please add local sales tax. McGraw-Hill pays regular shipping and handling on prepaid orders.

DCT


Loud and Clear
CVSD
PAGERS
VOICE MAIL
SATELLITES
VOICE/DATA MUX
PAIR GAIN
ENCRYPTION
HC-55564
Hearing is Believing
The new Harris HC-55564 CVSD offers you the ultimate in voice-band speech processing, compression and security. Its benefits include:
Low power CMOS
Real-time A to D
All digital
Few external parts
Commercial/mil packaging
Easy implementation
Low cost
Quick delivery
Harris provides you with demo boards and full applications support. So put our CVSD to work in your voice systems today. You'll hear the difference!
Contact: Harris Systems Ltd., European Semiconductor Operations, Eskdale Road, Winnersh Workingham, Berkshire RG11 5TR, England.
HARRIS TELECOM
HARRIS
For your information, our name is Harris.

Circle 88 on reader service card

SECOND ANNUAL IC ASSEMBLY AUTOMATION CONFERENCE

January 8 & 9, 1986
Red Lion Inn
San Jose, CA

ICAAC '86 will again bring an in-depth look at the advances made in assembly automation and process.

FOUR TECHNICAL SESSIONS

Learn from 16 papers which will address advances made in equipment, material effects on automation, practical lessons learned from automating and the CAM and CIM process.

EXHIBITS

See the latest in automated equipment, hardware and software. Learn about new materials and services.

KEYNOTE SPEAKER

Dr. Barry Johnson, Professor, University of Arizona
"Future Trends in IC Packaging."

COST: $225 If received before 12/15
$275 After 12/15 or at the door

Includes 2 lunches, cocktail party, technical sessions, exhibits.

EXHIBITS ONLY: No charge. Call to register.
REGISTRATION: Malka Nagel, INTEM, (415) 595-2803.
POB 390207, Mt. View, CA 94039

Circle 89 on reader service card

PROBING THE NEWS

JAPAN AND KOREA: OLD ENEMIES UNITE TO COMPETE

A MARRIAGE OF CONVENIENCE AIMS AT MUTUAL PROFIT

by Michael Berger

SEOUL

South Korea and Japan, which have have been at each other's throats more often than not over the years, are forging a marriage of convenience that is profiting electronics companies in both countries.

It's not an altogether smooth relationship. One Korean complaint is that Japan is reluctant to transfer technology. The Japanese, for their part, fear that the technology would be used against them in competition for world markets.

Whatever the emotions involved, some industry observers consider the unlikely alliance the future course of the international electronics-production business. And a clear picture of that course can be seen in Chuan, a suburb of Seoul, at Daewoo Telecom Co.'s plant.

On the Daewoo production line, workers are assembling Korean-designed personal computers fitted with a high ratio of components from Japan. They will be shipped to a U.S. customer, Leading Edge Hardware Products Inc. in Canton, Mass.

The personal computers have been a boon for Daewoo Telecom. Its computer division accounted for just 10% of total sales and perhaps $2 million in exports last year; it will bring in close to 45% of the company's estimated $80 million in sales this year. About $45 million of that total will be in exports (100% of computer sales are exports), says executive vice president Sung Kyou Park. He expects company sales to grow to $150 million in 1986, driven by the success of its 16-bit IBM-compatible personal computer, the Model D. The Daewoo-designed unit, priced at $1,495 complete, sells for about half the comparable IBM model. To meet demand, Daewoo's line is turning out close to 15,000 units a month.

Park says he isn't happy with the degree of dependence his company has on foreign suppliers for Model D components. But the fact that Daewoo can design and assemble such a product and make a profit vividly illustrates how Japanese and Korean companies already are finding ways to do business that is profitable to both sides.

The Model D's floppy disks come from Toshiba Corp., the keyboards from Alps Electric Co., and the power supply from DC Pack Co.—all companies with Tokyo headquarters. The hard-disk drive comes from Miniscribe Corp., Denver. About 80% of its integrated circuits are foreign-sourced, and 40% of those, says Park, come from Japan.

A GROWING LINK. The success of the Model D is just one example of a Japan-Korea electronics link that is growing impressively despite bitter emotions connected with Japan's occupation of Korea from 1910 to 1945 and a Japanese trade surplus with Korea that topped $3 billion last year.

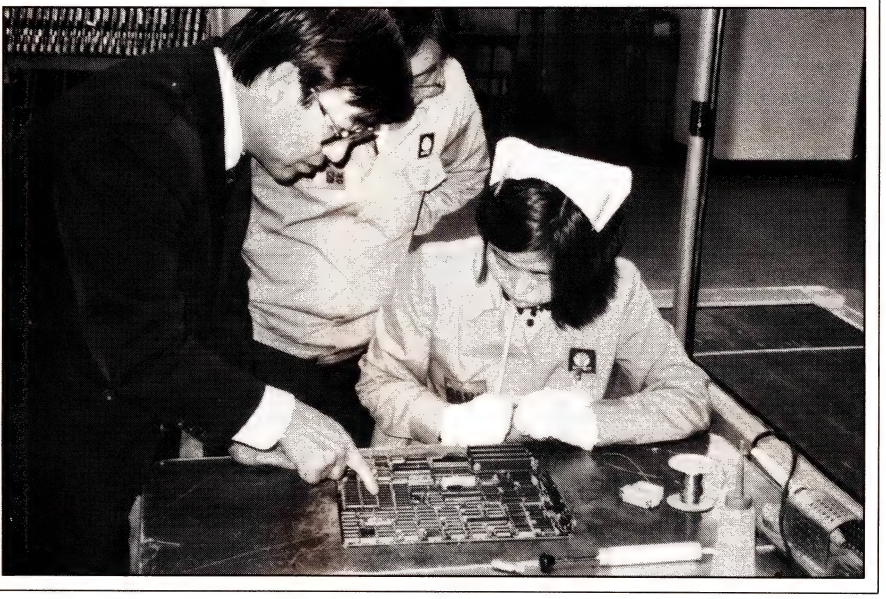
Japan's cumulative investments in Korea exceeded $1 billion in 1984 (see top table), a year in which Japanese companies signed 215 licensing agreements with Korean firms, more than double the overall U.S.-Korea total. Japanese and Korean companies, moreover, are moving toward a number of long-range tie-ups for production and marketing.

Virtually every Japanese electronics company has licensed technology to Korean firms within the last five years (see bottom table), and some second- and third-tier makers, such as Tokyo's Akai Electric Co., even have contracted Korean companies to supply them on an original-equipment-manufacturer basis. Akai and Samsung Electronics Co. of Seoul signed an agreement earlier this year whereby the Korean company is producing color TV sets for Akai to sell in Australia.

Other Japanese companies, such as Sony Corp., have equity interests in Korean producers. Many of Sony's compact stereo radio cassette recorders and portable radios are produced by Korea Sowa Corp. for reexport to foreign markets. Toshiba, which has a 6.5% interest in Korea Electronics Co., Seoul, and Hitachi Ltd., which has a working agreement with Tokyo Sanyo Electric Corp.'s Korean affiliate, both import a limited number of transistors, diodes, and other components. And as Korean makers improve their economies of scale on these and other products, they expect orders from Japan to increase.

The first of the major Japanese con-

BOARD MEETING. Daewoo Telecom's Sung Kyou Park with pc-board assembly workers.



sumer electronics companies to forge a long-range marketing pact might be Matsushita Electric Industrial Co., which has been talking to the Lucky Gold Star Group and other Korean makers about cooperative production arrangements. Matsushita's agreements with Korean companies so far are limited to production-technology transfers. But it seems only a question of time until the combination of lower Korean production costs and Japanese quality control and marketing skills adds up to a number of joint ventures that will be profitable for both sides.

Other examples of the Japan-Korea connection have been appearing almost weekly. This month alone, Fujitsu Ltd. licensed its electronic-banking-system software to Daewoo Electronics Corp., a sister company of Daewoo Telecom, and negotiated an agreement making the Japanese firm the main supplier of components for the Daewoo-built systems.

Hitachi Cable Ltd. announced that it and the giant construction firm Hyundai Corp. had landed a $3.5 million contract for an optical-fiber telecommunications network in Saudi Arabia, where the Korean firm has deep connections. Just a few days earlier, Sanyo Electric Co.'s trading subsidiary disclosed that its Korean joint-venture company will begin making compact-disk players for sale in Canada under the Fisher brand name.

NO LOVE LOST. Still, the main focus of Korea-Japan economic relations has been on the abrasions in the relationship. "They want it all to themselves, but they know it can't last forever," one Korean executive says of the Japanese. "That's why they license to us bit by bit, trying to keep us dependent on them for component supplies."

Other Korean executives see a more mutually profitable relationship emerging. "You don't have to love each other to do business," comments a Korean banker. "Older Koreans, even though they suffered under the Japanese occupation, still speak Japanese and understand them much better than they do the Americans or Europeans. Even younger Koreans, who may have a preference for the Americans, often wind up doing business with the Japanese, because they're more reliable."

"I've asked any number of American companies to send over their applications engineers for a seminar on their product or system," says Daewoo Telecom's Park. "They always say, 'Great idea,' but nobody's done it yet. With the Japanese, you don't even have to ask. They're on the way—and when you establish a relationship, they offer to let our engineers spend time in their laboratories."

On the Japanese side, ask executives about the South Koreans and within minutes they will be talking about "the boomerang effect," the fear that whatever technology they share with the Koreans will come back to haunt them in the form of competitive products. Many Japanese executives even see a "Korean-American" strategy of using lower Korean production costs and U. S. technical know-how to make products that will win market share from Japan.

To balance the dependency and keep the Korean connection growing and healthy, the Japanese must face up to some hard decisions. Koichi Yamaura, director of trade policy for the Ministry of International Trade and Industry's North Asia Division, warns that "Japanese companies should avoid talking vaguely about the boomerang effect, and develop strategies bearing in mind the long-term merits of building cooperative ties with South Korean firms." □

JAPANESE ARE TOP FOREIGN INVESTORS IN KOREA ($ millions)

Country	1962–81	1982	1983	1984	Total
Japan	633.3	42.6	167.5	163.8	1,007.0
U. S.	310.3	107.6	53.4	191.0	662.3
Europe	177.9	9.8	23.4	49.8	260.9
Others	127.1	27.8	23.5	14.4	192.8
Total	1,248	187.8	267.8	419.0	2,123.0

SOURCE: SOUTH KOREA MINISTRY OF FINANCE

TECHNOLOGY TIE-UPS BETWEEN JAPANESE AND KOREAN MAKERS

Japanese firm	Korean firm	Product or technology
NEC	Gold Star Electric	facsimile, telecommunications
	Samsung Electron	CRTs
Fujitsu	Daewoo Telecom	Korean-language version of FACOM 9450-II personal computer
	Dong Hwa Electronics (Fujitsu owns 19.8%)	
	FKL Dong Hwa (joint venture)	
	Jeil Precision	Korean-language version of dot-matrix printer
Toshiba	Samsung	word processors, microwave ovens, work stations
	Samsung	microwave ovens
	Daewoo Electronics	VCRs
	Korea Electronics	linear ICs, TV transistors
	Gold Star SSC	X-ray diagnostics
Hitachi Seiki	Kia Auto	flexible manufacturing
Hitachi	Lucky Gold Star	magnetrons
Matsushita	Lucky Gold Star	color TVs
	Samsung	microwave ovens
Akai Electric	Samsung	Samsung provides Akai with color TVs to be test-marketed in Australia; Samsung gets Akai technology for VCR magnetic heads
Yamatake-Honeywell	Gold Star Honeywell	interest in Gold Star Honeywell, licenses production control
TEAC	Oriental Precision	floppy-disk-drive production
Dainichi Kiko	Samsung Precision	robot production
Ricoh	Hyundai Electronic Industry	silicon wafers
Japan Victor	Samsung	VCRs
	Gold Star	VCRs
Sony	Samsung	compact-disk players 0.5-in. VCRs
	Gold Star	0.5-in. VCRs
	Daewoo Electronics	audio; 0.5-in. VCRs
	Korea Toyo Radio (owned by Sony)	Walkman headphones, radio cassette players for foreign markets
	Korea Sowa (Sony owns 50%)	low-end audio
Sumitomo Electric	Daehan Wire/Cable	fiber optics
Canon	Lotte	copiers

SOURCE: *ELECTRONICS*

PERKIN-ELMER UNLEASHES ITS DATA SYSTEMS GROUP

NEWLY INDEPENDENT CONCURRENT COMPUTER CORP. PLANS TO BUILD ON ITS PAST MINICOMPUTER SUCCESSES

NEW YORK

It is not always easy for a corporation known as a market leader in one or two categories of electronic products to be recognized as a leader in a different market. Perkin-Elmer Corp., a Norwalk, Conn., leader in analytical equipment and semiconductor-production gear, faced this problem with its Data Systems Group, which makes 32-bit superminicomputers.

As a division of a large corporation, the group was relatively unnoticed in the industry and often constrained by its parent's corporate management style and structure. To give its computer division more visibility and a more free-wheeling style, Perkin-Elmer two weeks ago set up a completely new company—Concurrent Computer Corp.—which will assume all operations of the Data Systems Group. Eventually, Perkin-Elmer will sell some of the new company to the public.

Perkin-Elmer believes Concurrent can be successful in the superminicomputer market, especially in the parallel-processing niche. And it believes that as a separate company, it will garner greater visibility in both the computer market and the financial community.

Concurrent's executives believe it has a huge head start on the competition—mostly startups—in the nascent market for parallel-processing machines. And industry analysts, who admit they don't follow Perkin-Elmer's computer operations closely because of its link to the parent, believe the strategy—and Concurrent's product line—will succeed.

"This is not a move from weakness. We're doing this because [Data Systems'] business is good and Concurrent is in a strong position," says Perkin-Elmer chairman Horace G. McDonnell. "It's necessary for [Concurrent] to be perceived as a pure-play player in the computer market."

Perkin-Elmer is "a leader in analytical equipment and semiconductor processing equipment, but these are small markets, whereas the computer industry is much bigger. We are the trendsetters in the first two," McDonnell says. However, these businesses require a somewhat conservative management style, one that is "inconsistent with the need to be a free-wheeling computer company."

"They're the only minicomputer company with rising sales; they are the granddaddy of the high-performance minicomputers; and they have more parallel-processor systems installed than anyone else," says James Wolpert, a market researcher at L. F. Rothschild, Unterberg, Towbin in New York. "They're serious about the business and are really bearing down on it."

In setting up Concurrent, Perkin-Elmer sold 1% of the new company's stock to eight Data Systems Group executives who together will run the new company. At their head is president James K. Sims, formerly a senior vice president and general manager of the Data Systems Group. Concurrent maintains its headquarters and manufacturing facilities in Holmdel, N. J., and has a plant in Cork, Ireland.

Concurrent's managers have options to purchase another 9% of Concurrent's stock from Perkin-Elmer. In addition, Perkin-Elmer plans to offer stock in Concurrent to public shareholders, although it plans to retain an 80% equity position in the computer maker.

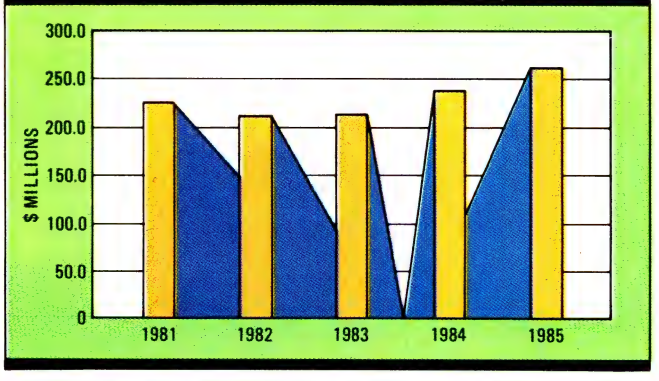
NOT PART-TIMERS. McDonnell points out that since 1974, when Perkin-Elmer entered the computer business through its acquisition of Interdata Corp., "we've been trying to get recognized as a member of the computer industry. We're perceived as a part-timer. We're anything but a part-timer," he emphasizes.

Rich Edwards, who follows the computer industry for Robertson, Colman & Stephens, a San Francisco investment banking and brokerage company, agrees that Perkin-Elmer has had a problem in this area. "They've always been thought of as a semiconductor-equipment company with some computer operations. From a buyer's standpoint, they're not sure what Perkin-Elmer's commitment is to computers, since it's not the largest part of the company."

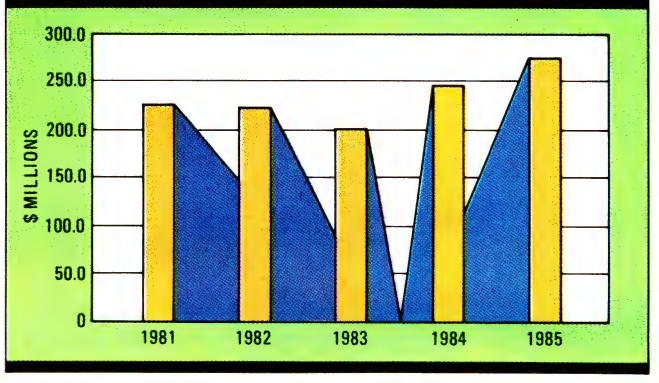
Concurrent starts out life in relatively strong financial shape. As the Data Systems Group, it had sales in fiscal 1985 of $259 million, up from fiscal 1984's $233 million. In addition, orders and pretax operating profit are on the rise (charts). Perkin-Elmer as a whole had total sales in fiscal 1985 of $1.3 billion, up from fiscal 1984's $1.2 billion.

"It will be a strong company," McDonnell says of Concurrent. "It will be

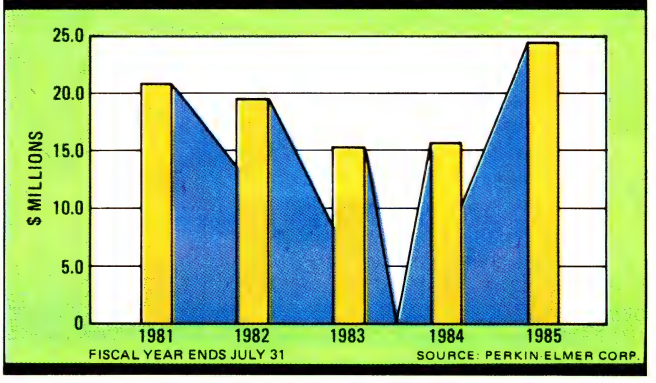
CONCURRENT'S SALES ARE UP . . .



. . . ORDERS HAVE INCREASED . . .



. . . AND PRETAX OPERATING PROFIT HAS GAINED



capable of being a self-standing company," rather than just a division of a larger corporation. He adds that Perkin-Elmer has no plans to invest further funds in Concurrent. "They have the internal cash flow to fund themselves."

That strength has come after a period of reorganization at the Data Systems Group, Sims says. Two years ago, the company pared the overhead in its operations. The division cut into its marketing and distribution organizations, he says, "and we took the money we saved and put it mostly in research and development so we could be on the cutting edge of the technology."

HEAD START. Concurrent Computer chief Sims says it has a track record.

"Our belief was that the 32-bit-computer industry would slow its growth and that the organization we had in place would have difficulty responding to that. We felt we had to reorganize, to become lean and mean," Sims points out.

He admits that the Data Systems Group never expected this year's downturn in the computer industry to be so severe. "But the structure of our company enabled us to stay profitable. We generated substantial profits for the company," Sims says.

Fast, affordable parallel processors are a specialty

To augment its solid financial footing, Concurrent also has a strong product line, especially in parallel processing. Here, its efforts are spearheaded by the 3280MPS [*Electronics*, Sept. 16, 1985, p. 52]. Touted as the company's highest-performing parallel-processing computer, one six-processor 3280MPS system offers six times the performance of a Digital Equipment Corp. VAX 8600 at comparable cost. "Parallel processing has become an important part of the computer industry and we have the leadership in that market," McDonnell says of the new company.

"Some fairly sophisticated users have gone with their systems," says Edwards of Robertson, Colman. He cites Singer Co. in flight simulators and the National Aeronautics and Space Administration. "They are the product leaders [in parallel processing] and have an excellent price-performance ratio on a mips [millions of instructions per second] basis. The 3280 is another big step forward."

The Data Systems Group's work in parallel processing stems from its earlier work in 32-bit superminicomputers, especially in its use of shared-memory architectures, Sims says. To meet the demands of users in the early 1970s, he says, most minicomputer companies opted to offer multifunctionality using 16-bit technology and sophisticated memory-management schemes.

"We came out in 1975 with the industry's first 32-bit minicomputer," says Sims. "It was a more difficult decision, but it let us prepare for larger growth." The company's early 7/32 and 8/32 Shared Memory Systems offered the earliest applications of parallel processing—letting different processors handle different parts of the same problem. These were followed by the Series 3200 Shared Memory System, and then the 3200MPS systems.

"The only competition that is surfacing [for Concurrent's parallel-processing equipment] is from a series of startups, not from the established competitors. A lot of [startup] companies are talking about neat architectures but are not making any money," Sims says.

"What the startups are delivering now, we've been delivering for a long time," he continues. "Why would a customer buy from them instead of from an established company with $200 million to $300 million in sales?

"We are a new company, yet we are well established," says Sims. "We have a new image but also a proven track record. We have a leadership position in parallel processing and we will continue the growth of the past." He says Concurrent will work to expand the sales of its computer systems to the commercial, industrial, and scientific communities.

Edwards of Robertson, Colman concurs. "The resources of Perkin-Elmer put [Data Systems Group] in good standing versus the smaller companies," such as Ridge, Pyramid, and Elxsi. These are companies with good superminicomputers but without the backing that the Data Systems Group had."

Concurrent has another advantage over the Data Systems Group when it comes to attracting employees, Sims says. "Computer people like to work for computer companies, not conglomerates. Concurrent will be better able to attract people with stock options and stock purchase plans." *–Robert J. Kozma*

BOTTOM LINES

AMERITECH TO BUY ADR FOR $215 MILLION

Ameritech, one of the seven regional Bell operating companies that were created by the breakup of AT&T Co., has agreed to acquire Applied Data Research Inc., a developer of software for use on IBM Corp. computers. Ameritech, Chicago, has agreed to pay $32 a share, or a total of $215 million, for the Princeton, N.J., company. Ameritech said it would pay for the acquisition with internally generated funds. As of Sept. 30, it had $413 million in cash and short-term investments.

3M TO ACQUIRE COMPONENT LINES

In an effort to broaden its cable and connector business, 3M Co., St. Paul, Minn., has agreed in principle to acquire some of the businesses of Associated Enterprises Inc., Painesville, Ohio, for an undisclosed amount. The businesses include the Aptronics and AP Products connector lines and the Symbex and Chabin cable products. They will become part of 3M's Electronic Products Division, Austin, Texas. The new businesses fit with the company's existing businesses, says a 3M representaive, "and with our strategic plans to broaden the line of products we offer to the worldwide electronics industry."

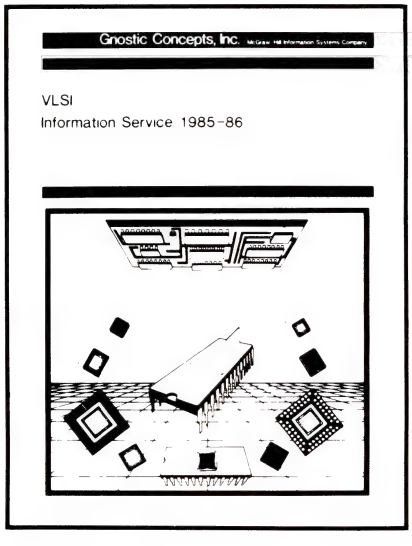
MICRON TECHNOLOGY INVESTS IN ASICs

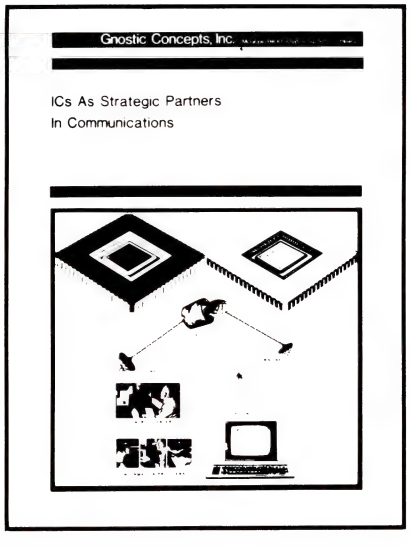
Micron Technology Inc., a Boise, Idaho, maker of dynamic random-access memories, has invested an undisclosed amount in Barvon Research Inc., a 3½-year-old privately held company in Milpitas, Calif. Micron said that under the investment agreement, it will own 800,000 shares, or about 20%, of Barvon, with an option to buy up to 50% within two years. According to Micron, Barvon Research designs and sells application-specific chips, specializing in high-speed digital and mixed analog-digital standard-cell integration.

MAGNESYS GETS VENTURE CAPITAL

Magnesys, a startup with plans to build proprietary bubble-memory systems, has received $2.75 million in venture-capital financing. The San Jose, Calif., company hopes to be bringing its products to market within one year, saying it will "pursue the market for bubble-memory products targeting end-users with fully integrated, off-the-shelf system products."

STRENGTH THROUGH KNOWLEDGE





Semiconductor industry and markets

– An annual subscription service

ICs and communications systems pace one another in technological development

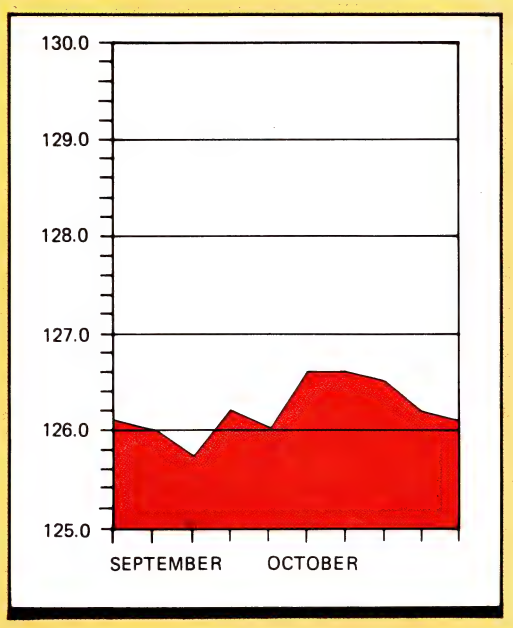
– A new multiclient study

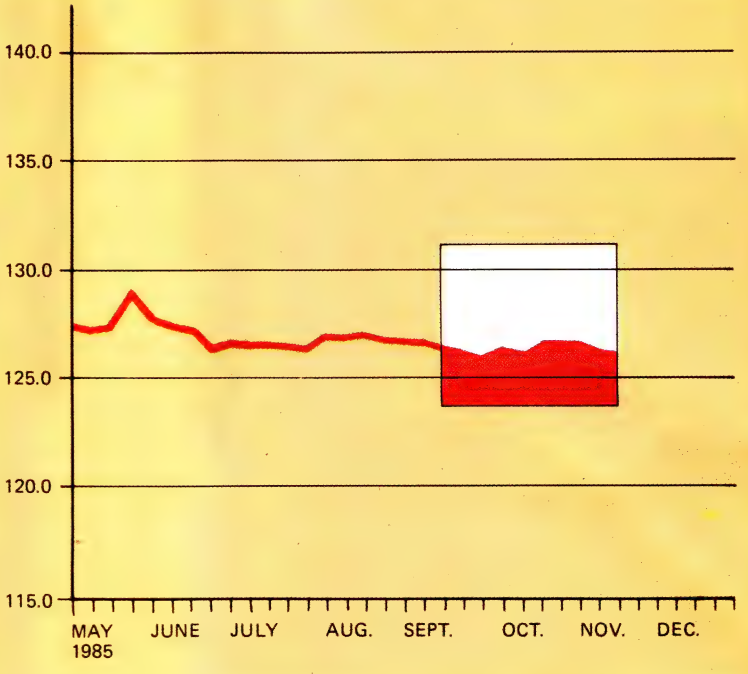
Quality market research information and services

. . . . . knowledge, it's in our name. Gnostic Concepts, Inc.

951 Mariner's Island Boulevard Suite 300 San Mateo, CA 94404
Telephone 415/345-7400 TWX (910) 374-3019 (GNOSTIC SMT)

ELECTRONICS INDEX





THIS WEEK	= 126.1
LAST WEEK	= 126.2
YEAR AGO	= 133.3
1982	= 100.0

The *Electronics* Index, a seasonally adjusted measure of the U.S. electronics industry's health, is a weighted average of various indicators. Different indicators will appear from week to week.

U.S. IMPORTS & EXPORTS ($ MILLIONS)

	IMPORTS			EXPORTS		
	September 1985	August 1985	September 1984	September 1985	August 1985	September 1984
Accounting, computing, and data-processing machines	315.224	268.382	448.749	553.163	533.565	612.345
Calculators	60.012	40.556	32.191	5.467	4.984	8.717
Parts for data-processing machines and office calculators	375.077	348.916	385.340	519.635	531.275	580.389
Telecommunications, sound-recording, and sound-reproducing equipment	1,719.462	1,516.636	1,499.796	338.173	297.060	298.380
Electronic or electric instruments	159.046	141.302	110.323	503.443	502.773	509.104
Printed-circuit boards	28.085	24.511	25.246	23.137	22.109	24.528
Integrated circuits, diodes and other semiconductors, tubes, piezoelectric crystals, parts	492.345	446.224	744.669	327.491	344.715	469.595
Fixed and variable resistors	18.590	16.000	25.731	11.822	11.034	13.890

An unfavorable trade picture for electronic equipment in September helped push the *Electronics* Index down a notch and heightened doubts that the U. S. electronics industry will soon regain its historically dominant trade balance. Imports of electronic equipment scored a 13% gain in September, according to the latest government statistics, while exports inched up a feeble 1.5%. As a result, the U. S. electronics industry's trade deficit ballooned 60% from a year ago, to $886 million. The villain behind the trade debacle, the U. S. dollar, shows no sign of significant weakening in the near term.

Despite the overall lackluster results in electronics trade in September, some market segments were strong performers. For example, exports of telecommunications equipment were up 14% in the month, and calculator exports increased 10%. On the downside were exports of parts for computers and other office equipment, which fell 2.3%. International markets for components remain weak; domestic manufacturers experienced a 5% drop in exports in September. And though imports of foreign-made components increased more than 10% from the previous month, they were still 34% below levels of a year ago.

VANDER DUSSEN IS AIMING SONY TOWARD FLEXIBILITY

PARK RIDGE, N. J.

Japanese companies have a tradition of using the best ideas or people they can find to enhance their competitive position in world trade. Sony Corp. is hoping that the new president and chief operating officer of Sony Corp. of America, Neil Vander Dussen, will help revitalize this important arm by cultural cross-pollination—instilling some Yankee entrepreneurism.

Vander Dussen's task is to cut away the excess bureaucracy that can choke new ideas and awaken in Sony America executives an independent attitude that will allow them more creative latitude. To that end, he has developed a new managerial hierarchy with Kenji Tamiya, the new chairman and chief executive of Sony America.

Sony broke down its Consumer Products Co. and Communications Products Co. into eight distinct product divisions early this month. "We changed the organization by structuring it with more individual business units," Vander Dussen explains. "We delegated more responsibility and more authority to the heads of those units so that they could reach their objective—to continue to grow and to be more responsive to the marketplace. We have a flatter organization now, with fewer levels of management."

Vander Dussen cut two management tiers, assuming supervisory responsibility for those product divisions and three companies—Broadcast Products, Magnetic Products, and Service. The three companies are self-sufficient with their own sales, financial, advertising, and marketing staffs. The divisions, however, are sales and marketing organizations only and depend wholly on the parent company for those other services.

The executive also plans to institute a new kind of corporate incentive program for Sony employees, though he declined to elaborate. "We want to further stimulate the entrepreneurial attitudes that tend to make a business grow faster," Vander Dussen says.

Vander Dussen, who holds a BSEE from Kansas State and an MS in management from Massachusetts Institute of Technology, spent 25 years with RCA Corp., a career that ranged from salesman to executive vice president of the Commercial Communications Systems Division. "I have a great deal of respect for that company," he says, but he saw in Sony a company that was more intriguing, with qualities that were not dominant at RCA.

"Sony is a company that invests a great deal in technology. It has a unique ability to select technologies to be used in products and has the willingness to introduce those products into brand-new markets. It is a company with a great deal of vitality."

Vander Dussen signed up as president and chief executive officer of Sony Broadcast Products Co. in 1981 and has gone through jobs the way some people trade in cars—almost on an annual basis. In 1983, he was named president of the Consumer Products Co.; in 1984, president of Sony's U. S. Marketing Group. Smiling, he refuses to speculate on what he will be doing in 1986. *–Tobias Naegele*

SLIMMER. Vander Dussen is paring Sony's excess bureaucracy.

PEOPLE ON THE MOVE

REX L. JAMES

☐ Rex L. James, a 22-year veteran of Hewlett-Packard Co., Palo Alto, has taken over the reins as general manager of the company's Greeley Division, which produces data-storage devices for personal computers. Previously operations manager for the Personal Mass Storage Mechanisms Operation at the division in Greeley, Colo., for the past year, James has also held various positions at HP's Fort Collins Division. He holds a bachelor's degree from Brigham Young University and a master's degree from Colorado State University.

DAVID L. DALLOB

☐ David L. Dallob, a former staff vice president of Sperry Corp., is now aiming to make advanced manufacturing systems a strategic resource for Varo Inc. Dallob joins the defense electronics company in Garland, Texas, as vice president and chief operating officer. His appointment is part of a major realignment of senior management, which, according to Varo president James F. Gero, is geared toward reaching a goal of $300 million in revenue by the mid-1990s. Also joining the company is Kevin McAleer, former vice president of Tocom Inc. in Irving, Texas. McAleer becomes Varo's chief financial officer in December, replacing Clifford L. Steward, a vice president who will assist in negotiations for future acquisitions and possible joint ventures. Herman Albertine, who has been general manager of Varo's Electro Devices Division, is now general manager of ITT/Varo, a joint venture formed last June with ITT Corp.

JOHN W. SMITH

☐ With Dallas Semiconductor Corp. moving into the volume-production phase, the 22-month-old startup has promoted its cofounding vice president of manufacturing, John W. Smith, to president. Smith, 41, fills the position that was held by venture capitalist Vin Prothro. Prothro remains as chairman. Before helping to start Dallas Semiconductor, Smith was Mostek Corp.'s facilities director for plants in Texas, Colorado, Ireland, and Malaysia. He also had worked six years for Texas Instruments Inc., where he supervised the design and construction of two automated wafer-fabrication lines.

KENNETH B. FINE

☐ As former general manager of Intel Corp.'s microprocessor division, Kenneth B. Fine oversaw the introduction of the company's new 32-bit microprocessor, the 80386. As the new president of Valid Logic Systems Inc., San Jose, Calif., Fine may be looking at microprocessors differently—in this case, selling the sophisticated design systems used to create the chips. Valid is looking for Fine's experience in marketing to major corporations to help the company fight the eroding market share of its computer-aided-design and -engineering tools based on AT&T Co.'s Unix. Before working at Intel, Fine held various positions at Digital Equipment Corp. He received his bachelor's, master's, and doctorate from the University of Illinois.

NOW PENISTEN MANAGES SEED-MONEY FUNDING

MENLO PARK, CALIF.

Glenn E. Penisten, the semiconductor-industry veteran who engineered a legendary turnaround at American Microsystems Inc. in the late 1970s, has turned to starting companies instead of saving them. Penisten joined the venture avant-garde in September as a general partner in Alpha Partners, a three-year-old specialist in seed money.

Alpha, a $40 million fund started by Wallace F. Davis, who funded the successful Mayfield venture fund 16 years ago, shuns massive venture investments. Instead, it tries for a high rate of return on relatively little seed money to help get companies to the place where they can start to attract second-round venture funding. For instance, one of Alpha's companies is designing a process for wafer-scale integration of semiconductors.

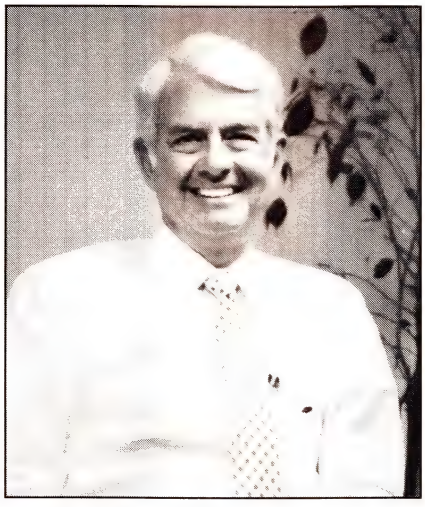
Alpha might put up the first $100,000 to complete a business plan and hire a chief executive officer; and, to carry a company through its first product delivery, it might put up $2 million or more. At some point, it would retreat from active direction of the company to an advisory role, guiding it through two or more rounds of venture financing and then retrieving its investment when the company is acquired or goes public. Its targeted return is 40%.

FILLING A NEED. The appearance of seed funds reflects the maturity of the venture market, Penisten says. "High technology makes it possible to take an idea and build it into a company in a very short time. Commercial banks couldn't handle that and the venture funds sprang up. Today, with technology changing everywhere, even the venture capitalists need to be more careful. They want to know if there is a market study and a business plan, and who is the vice president of marketing."

Alpha performs those services, acting as a pre-venture capitalist. It will invest the cash and provide the expertise to make a startup appeal to venture money. Davis and Penisten screen proposals and then raise the money. Despite the recent electronics industry downturn, "there's as much action now as there ever was," according to Davis.

Penisten, 53, provides the kind of management strength seldom available to startups. At 35, he was a corporate vice president at Texas Instruments Inc., where he founded the consumer operation and directed worldwide semiconductor marketing. Later, he rescued AMI from near extinction and rebuilt it to the point where Gould Inc. bought it for $237 million in 1982. After that, Penisten ran several other Gould companies and even considered the presidency of Gould itself. But "I decided I had no more to prove running companies."

Penisten then tried investing in companies himself. One of them was Inova Microelectronics Corp. of Campbell, Calif., which is developing a proprietary method of interconnecting chips on a wafer. Alpha had provided the seed money for Inova.



PLANTER. Glenn Penisten has gone from turning companies around to seeding them.

Davis saw that Penisten's experience could bring managerial strength to Alpha, and his high visibility—he serves on many boards of directors and in 1983 was chairman of the American Electronics Association—would help raise money. "He's an ideal addition to Alpha," says Davis.

MADE, NOT BORN. Penisten says Alpha's approach makes more sense than just hunting down good business plans. "Companies are made, not born," he contends. The process begins with a market study to determine whether the venture is even feasible. The answer may have nothing to do with current market conditions.

In fact, adds Penisten, economic slumps such as the one currently afflicting the semiconductor industry can provide the best opportunities for starting companies "because the creative people aren't getting their bonuses."

"The semiconductor market is dead right now," says Penisten. "But we've still got 12 months of design work to do anyway." *–Clifford Barney*

GRAMMAR ENGINE

Providing Ruggedness and Uncomparable Reliability in

COMMUNICATIONS HARDWARE

Designing Products used by The Government, Military and Fortune 500 Companies.
Products like COMBOARD Unibus, Al-170
Data-Pbx, MACH1 Multibus communications slave.
Available in Jan. '86, MACH2 a 4Mbits serial link on Multibus and other bus environments.
MC68000 based, 3 yrs Warranty

Grammar Engine, Inc. 1021 Tipton Ct.
Westerville, Oh 43081 614 882 6366

Circle 69 on reader service card

A guide to semiconductor strategies in the 80's!

CUSTOM & SEMICUSTOM VLSI: Survival Strategies For The New Era asks the question: Are you equipped to meet the challenges of an ever-changing industry?
Radical change in industry can mean radical growth if you understand these changes.

Order this book today for an inside line on the challenges of change in the semiconductor market.

Send $150 or your company purchase order to: R360

Electronics Books
P.O. Box 541
Hightstown, NJ 08520

SALES REPRESENTATIVES WANTED

Representatives wanted in all territories for bench and rack mount power supplies. Contact:

R. Robinson
Brunelle Instruments, Inc.
P.O. Box 745
Newport, VT 05855-0745
(819) 563-9096

COMPUTER SOFTWARE

SPICE up your *PC*

Z/SPICE professional circuit simulation
Full version $245 Student version $79
ZTEC box 737, college place, wa 99362
(509)-529-7025

POSITIONS VACANT

Murkett Associates — Technical Mgmt placement with national affiliates-fee paid Box 527, Montgomery, AL 36101.

POSITIONS WANTED

I do microprocessor hardware/software, assembly language. Analog, digital design in my N.Y. lab or worldwide. Project rates. Mr. Barry Masel (718) 476-1516.

HOT LINE

To place your recruitment message in

Electronics

call Pat Clyne at

212/512-2557

Advertise your software for only $114.75

For only $114.75 per inch you can advertise your software, designed specifically for the electronics industry, to a no-waste audience specifically in need of it—Electronics' paid circulation of 102,000 subscribers.

You'll waste no advertising dollars on waste circulation. These decision-makers need software applications designed specifically for their industry. That's why Electronics' Computer Software Section is a perfect interface because it is programmed to connect you with specific industry interests.

Send your copy/art to the address below. For more information, call Patti Clyne at 212/512-2557.

Electronics Computer Software Section
Post Office Box 900
New York, NY 10020

1985 ELECTRONICS COMPUTER SOFTWARE SECTION

Sizes		Material
1 Inch	7/8 x 2 1/4	Artwork or
2 Inch	1 7/8 x 2 1/4	film preferred.
3 Inch	2 7/8 x 2 1/4	Typesetting
4 Inch	3 7/8 x 2 1/4	free of charge.

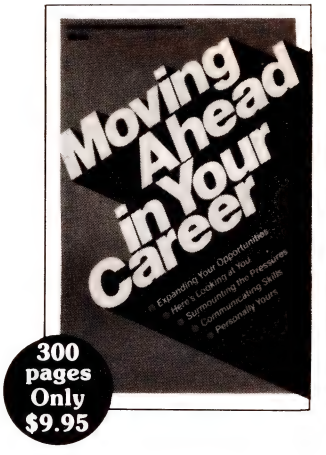
1985 RATES

Unit	1X	6X	12X
1 Inch	$114.75	$113.75	$112.80
2 Inch	229.50	227.50	225.60
3 Inch	344.25	341.25	338.40
4 Inch	459.00	455.00	451.20

Call Patti Clyne 212/512-2557

Are you in your first engineering job?

Are you thinking about where you go from here?



This book is a practical how-to-do-it guide from Graduating Engineer that you can put to use right now—articles like "How to Get a Good Performance Appraisal", "The Importance of a Mentor", "The Road to $50,000 a Year", "Winning at Office Politics"—and many more. Send for this book today and begin to move ahead in *your* career.

GRADUATING ENGINEER
P.O. Box 900
New York, NY 10020

Please send me ___ copies of "Moving Ahead in Your Career" at $9.95 each. Enclosed is my check/money order made out to Graduating Engineer for $_____

Name _____

Address _____

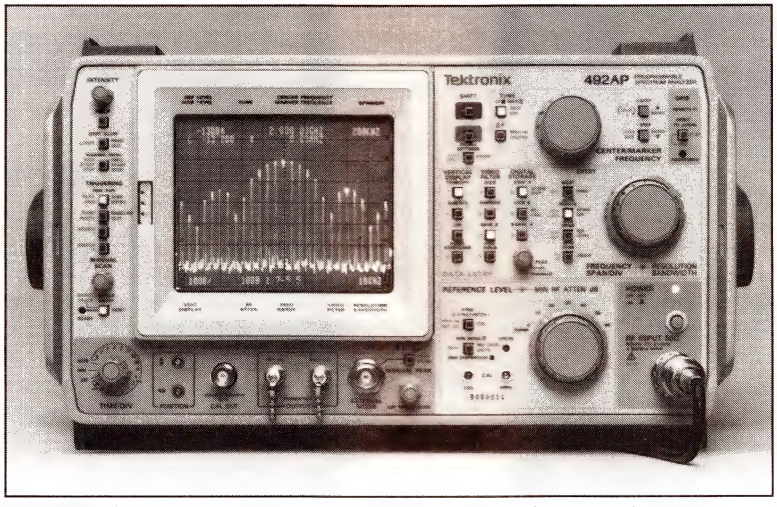
City/State/Zip _____ E

NEW PRODUCTS

PORTABLE ANALYZERS MATCH FEATURES OF HIGH-END MODELS

PROGRAMMABLE UNITS PERFORM INTELLIGENT PROCESSING

Tektronix' Frequency Domain Instrument Division has come up with a pair of portable spectrum analyzers—the model 492A, and its programmable twin, the 492AP—that boast a frequency range and level of intelligence typically found only in systems costing much more. The 492A covers 50 kHz to 325 GHz external-mixer input in one sweep. The center frequency range for direct coaxial input is 50 kHz to 21 GHz. Prices start at $27,290.



MARKERS. Tektronix' analyzer uses two smart markers for measuring traces.

Morris Engelson, manager of the Frequency Domain Instrument Division, says that customers have asked for a portable instrument in this frequency range and that Tektronix designed the 492A to answer that demand.

The 492A is identical to the higher-ticket model 494, except that it does not not have a frequency counter. In all other respects, the 492A offers the same speed, accuracy, and intelligence as the 494, including programmability—the 492AP interfaces with a host computer over the IEEE-488 interface bus.

ALTERNATE UNITS. All spectrum analyzer show amplitude, calibrated in dBm, versus frequency. On the model 492A, alternate reference units of dBV and dBmV are also available. Varying a local-oscillator frequency synchronized with the display's horizontal sweep gives the display's frequency dimension.

The 492AP has a number of intelligent features. The instrument's microprocessor performs intelligent signal processing for sorting continuous-wave pulses and spurious signals. Additionally, a single smart marker can be used for direct readout at any point on a displayed trace, or two markers can be used for finding the difference between two points on a trace or between different traces. In delta-marker mode, resolution is to within 100 Hz at a minimum.

The user can position the marker either by a knob or by a keypad entry. A sort-and-distinguish feature locates the main low frequency and side low-peak amplitude in two keystrokes using the signal-processing algorithm.

An occupied-bandwidth function automatically measures the occupied bandwidth following a sweep, at a user-determined level below the displayed peak of a marked signal. Built-in preselection eliminates harmonic mixing products and images and increases the instrument's dynamic range.

Ten nonvolatile memory locations store front-panel settings and waveforms—a feature that makes it easy to take measurements in the field and bring them back to the bench for comparison and analysis.

Controls are grouped logically and labeled clearly on the front panel. Another aid to the operator is Help-mode, menus that further explain the controls and all of the instrument's signal-processing functions.

Tektronix is not leaving the military out in the cold with this spectrum analyzer. A Mate/CIIL language option extends the IEEE-488 interface bus standard codes and formats for military applications, and an optional 75-Ω input is available for testing satellite uplinks and downlinks.

Both the 492A and the 492AP are scheduled for first shipment 12 weeks after receipt of order. *–Ann Jacobs*

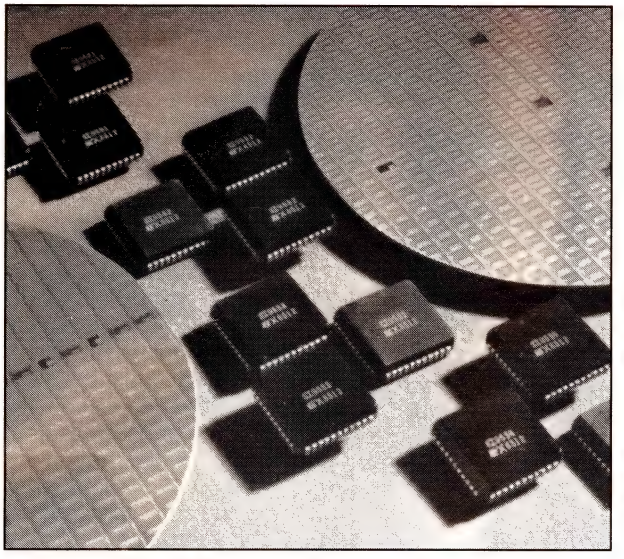
Tektronix Inc., Marketing Communications Department, P. O. Box 1700, Beaverton, Ore. 97005. Phone (800) 547-1512; in Oregon, (800) 452-1877 [Circle reader service number 339]

EL DISPLAYS GET BOOST FROM LOW-POWER DRIVERS

Siliconix' second-generation display-driver ICs could end the biggest challenge designers face when working with electroluminescent displays—driving the displays quickly but using little power. The chips, which are built in Siliconix D/CMOS Smartpower process, improve the performance of first-generation parts without increased cost.

"The drivers are about 50% of the cost of a flat-panel-display system," says William Numann, the company's power-IC product marketing manager. One of the ways Siliconix is keeping cost low is with the self-isolation process it uses: "You get away with the least costly method of isolation that works—in this case, self-isolation."

With the new row and column drivers, the designer can boost display brightness, sharpen resolution, and reduce overall power dissipation in an EL display. The drivers are pin-compatible with such first-generation 32-channel



BRIGHTER. Siliconix' new driver ICs make for brighter electroluminescent displays. Parts are available in chip carriers or as dice.

driver circuits as the SN75551 through SN75556 line, which Texas Instruments Inc. fabricates in Bid-FET process technology. In Bid-FET, CMOS logic controls double-diffused-MOS devices, which in turn drive bipolar power transistors.

The column drivers are critical to a display panel because they shift data in and out at very high speeds, says Numann. The 32-channel column drivers, part numbers Si9553, Si9554, Si9555, and Si9556, have a 10-MHz 32-bit shift register, 32-bit latch, and 32 totem-pole outputs rated at 60 and 90 V. TI's column drivers are rated at only 6.2 MHz. Siliconix' circuits have a sink-and-source capability of up to 15 mA over the commercial temperature range (0° to +70°).

Siliconix cut power consumption by an order of magnitude by using an active level-shifting technique. At the low end, Siliconix' parts are rated at 0.5 mA, compared with 5 mA for the TI parts, Numann says. He gives the ratings on the high end as 1 mA for the Siliconix parts and 10 mA for the TI versions. This means that Siliconix' drivers run much cooler, which gives a lower power dissipation for the display, Numann says. "Power consumption is a key consideration in portable applications."

The Si9551 and Si9552 are designed to drive the row lines of an EL panel. These 32-channel row drivers have a 32-bit shift register and 32 open-drain DMOS output devices rated at 225 V and 80 mA over the commercial temperature range. The row drivers are less critical to the display. "In the row drivers, we have improved by about 50% the output structure, providing a higher drain-current rating." TI's parts are rated at just 50 mA throughout the commercial temperature range, though a new TI series boasts ratings as high as 160 mA. The improved rating allows designers of electroluminescent displays to drive larger panels with improved brightness, Numann says.

Siliconix plans to introduce enhanced row and column drivers with increased voltage and current output capabilities based on its D/CMOS technology, which combines DMOS and CMOS transistors on the same die. The drivers come in ceramic quad 44-pin J-leaded packages, plastic quad 44-pin leaded chip carriers, or in chip form. In lots of 1,000 pieces, prices range from $5.40 to $29.02 each. The ICs are available now. –*Steve Zollo*

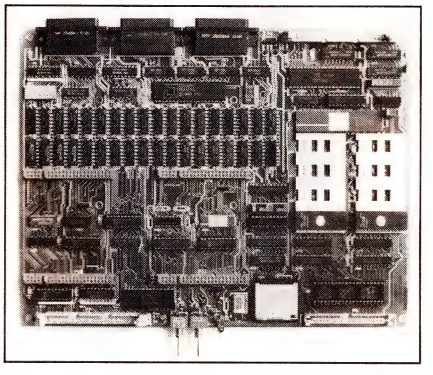
Siliconix Inc., 2201 Laurelwood Rd., Santa Clara, Calif. 95054.
Phone (408) 988-8000 [Circle 338]

$950 COMPUTER CARD IS BASED ON 80186

The VS-186 single-board computer creates an industrial or scientific system using PC-DOS at half the cost of a comparable Multibus or VMEbus system, the manufacturer says. Based on the 80186 microprocessor, the $950 board is fast and flexible—four iSBX expansion connectors accept daughter boards such as analog-to-digital converters and IEEE-488 interfaces.

With the VS-186, up to 512-K bytes of ROM can be installed in eight Jedec 28-pin EPROM sites. This allows construction of diskless systems by loading programs onto EPROMs. The board comes with up to 1 megabyte of parity-checked RAM; a socket is included for an 8087 math coprocessor.

The 8½-by-11-in. board has two serial ports, a programmable parallel port, a Centronics printer port, a SASI-SCSI interface for disk and tape drives, and a processor bus extension that allows communication with other bus structures. For operation in vibration-heavy, noisy industrial environments, all expansion connectors and cable jacks are provided with hold-down screws and positive shielding. The operating temperature range is 0° to 55°C.

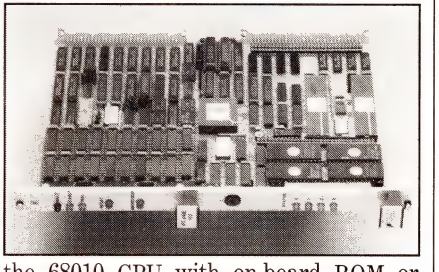


Virtual Systems Inc., 1500 Newell Ave., Suite 406, Walnut Creek, Calif. 94596.
Phone (415) 935-4944 [Circle 356]

COMPUTER CARD HAS 10 ADD-ON OPTIONS

The PT-VME102 is a single-board computer for the VMEbus that offers 10 different plug-in I/O configurations, called I/O Paks. With the I/O Paks, users can add up to six serial I/O ports with or without direct memory access, a Small Computer Systems Interface with or without DMA, a 68881 floating-point processor, and a Centronics parallel port. Additional I/O Paks will be available in the future.

The standard board comes with 512-K bytes of dynamic RAM that can be upgraded to 2 megabytes. This on-board memory features Multiport access, which allows concurrent operation of



the 68010 CPU with on-board ROM or module-based I/O while the VMEbus is accessing the DRAM. The board also includes a real-time clock with on-board battery backup, a VMEbus system controller, a seven-level interrupt handler, and two serial ports.

Pricing starts at $2,195 for a board with 512-K bytes of memory and I/O Paks sell for $200 to $895. Delivery takes four to six weeks.

Performance Technologies Inc., 300 Main St., East Rochester, N. Y. 14445.
Phone (716) 586-6727 [Circle 354]

MULTIBUS CPU SERVES 48 LINES

The CBC 85C/24 is an all-CMOS Multibus CPU card that puts 48 parallel I/O lines into service on the factory floor. It also features a programmable serial interface and two programmable 16-bit counter-timers.

The card, which operates at 150 mA

Toshiba DRAMs—the pick of the bunch.

Toshiba, the acknowledged world leader in CMOS and NMOS memory technology is up with the front runners in volume production of DRAMs.

We were among the first to introduce 256k DRAMs, and today we're a market leader. Our 1Mbit DRAMs in CMOS and NMOS are available now – another market leader achievement!

Our range includes 4 bit and 1 bit organisation parts with a variety of functions. Continuing development is constantly re-inforcing the line-up.

PART NO.	ORG	PROCESS	ACCESS TIME	FUNCTION
TMM4164AP	64k×1	NMOS	120,150,200nS	page mode
TMM41256P	256k×1	NMOS	120,150nS	page mode
TMM41257P	256k×1	NMOS	120,150nS	nibble mode
TMM41464P	64k×4	NMOS	120,150nS	page mode
TC511000C	1M×1	CMOS	100,120nS	fast page mode
TC511001C	1M×1	CMOS	100,120nS	static column mode
TMM411000C	1M×1	NMOS	100,120nS	page mode
TMM411001C	1M×1	NMOS	100,120nS	nibble mode

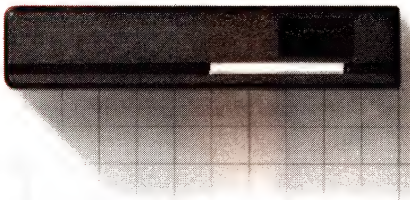
For futher information on DRAMs to fit your precise requirement, contact

TOSHIBA

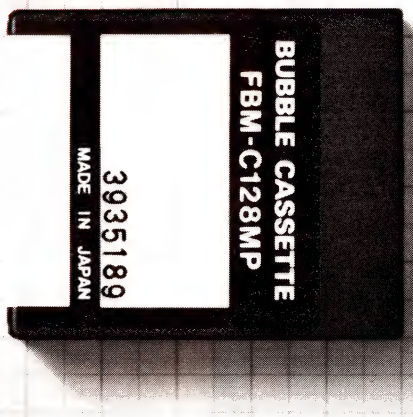
Toshiba Europa (I.E.) GmbH,
Hammer Landstrasse 115, 4040 Neuss 1,
West Germany. Telephone: (02101) 157 (0)

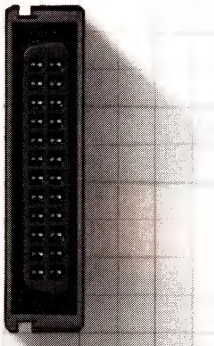
Circle 83 on reader service card

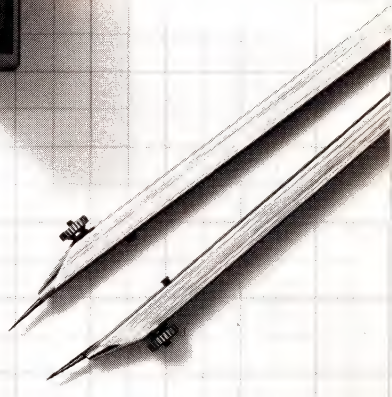
NEW



actual size

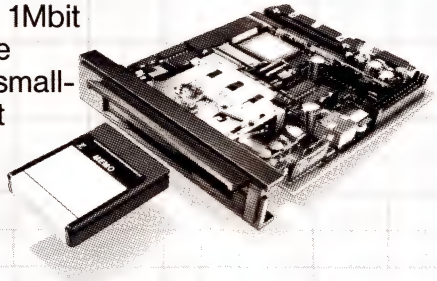






Smallest in size, bigger in memory.

Fujitsu introduces world's smallest 1M bit compact bubble cassette.



Fujitsu's unique 1Mbit compact bubble cassette is the smallest and thinnest memory of its kind in the world. It's also lightweight, easy to carry, dust-proof, shock-resistant and maintenance-free with no mechanical parts, so it's ideal for use in hand-held terminals of every kind. And it features a fast access time of 12.8ms and 8-bit parallel interface. For full details on this amazingly compact, high-performance memory system, contact the address below.

Major Specifications

Compact cassette	FBM-C128MP
Holder unit	FBM-U550GA
Memory capacity (user area)	
Data area	128K bytes (64 bytes/page x 2048 pages)
Sub-pages	192 bytes
Mean access time	12.8ms (2.6ms with SEEK command)
Interface	8-bit parallel (DMA capability)
Transfer rate	100K bits per second (max)
Transfer method	64 bytes block transfer
Dimensions	
FBM-C128MP	52(D) x 43(W) x 11(H) mm
FBM-U550GA	156(D) x 125(W) x 25(H) mm

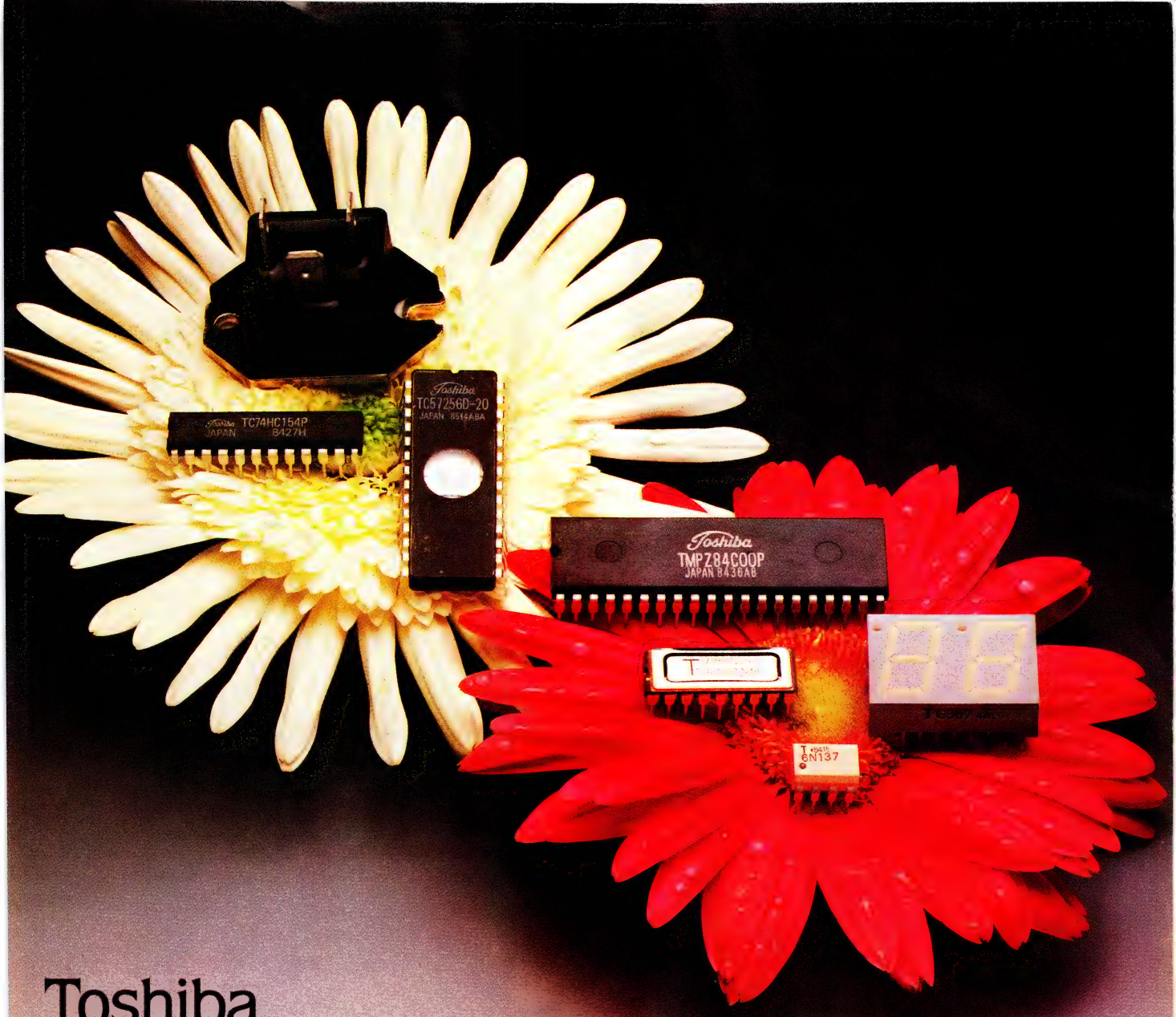
FUJITSU SYSTEM COMPONENTS

Fujitsu Component Europe, B.V.:
Rijnkade 19B, 1382 GS, Weesp, The Netherlands Phone: 02940-18748/18914 Telex: 11966 FUJCE NL

Fujitsu Component Europe, B.V. NIEDERLASSUNG DEUTSCHLAND:
Arabella Center, 12th Floor, Lyoner Str. 44-48, D-6000 Frankfurt/Main 71 Phone: 069-66320 Telex: 411963 FMG D

Fujitsu Limited (Components Marketing):
Furukawa Sogo Bldg., 6-1, Marunouchi 2-chome, Chiyoda-ku, Tokyo 100, Japan Phone: National (03) 216-3211
International (Int'l Prefix) 81-3-216-3211 Telex: 2224361 FTTOR J

FUJITSU



Toshiba semiconductors - the pick of the bunch

For many years Toshiba has been recognised as one of the world's leading microelectronics manufacturers. A volume producer of highly reliable leading edge designs, Toshiba has shown the way in CMOS technology.

But there is more to Toshiba than just microelectronics products. In fact, our whole line-up is constantly expanding to meet the challenge of a demanding industry.

Discrete semiconductors; Power devices; Opto products; Linear ICs; Dynamic RAM; NMOS and CMOS static RAM; Mask ROM; Microprocessors; Gate arrays – a truly comprehensive range, manufactured to the same high standards that built our microelectronic reputation.

Whatever your needs – discrete, bipolar or MOS – make it Toshiba. The pick of the bunch.

TOSHIBA

Toshiba Europa (IE) GmbH,
Hammer Landstrasse 115, 4040 Neuss 1,
West Germany. Telephone 02101 157 (0)

Circle 85 on reader service card

The Write Stuff

When you write your valuable data on disks, you want to be sure you get the right disk. The "brain cells" of our magnetic disks are special oxide particles so small and so extraordinarily uniform that we can create a very dense oxide layer to increase storage capacity. And our heat-resistant jacket protects your data against high temperatures, resists deformation, and has a special fabric liner that continually cleans the disk.

Every track of every floppy is certified error-free for all our 4 sizes: 8″, 5¼″, 3½″, and 3″. Say bye bye to dropouts and hello to reliability your data deserves. Maxell floppies are indeed the write stuff.

maxell®

When every bit counts, it's Maxell.

Hitachi Maxell, Ltd.: 3-3-1, Ginza, Chuo-ku, Tokyo 104 Phone: (03) 564-0801 Telex: J26391 MAXELL **Maxell Europe GmbH:** Emanuel-Leutze-Str. 1, 4000 Düsseldorf-Oberkassel, F.R. Germany Phone: (0211) 59510 Telex: 8587288 **Maxell (U.K.) Ltd.:** 1 Tyburn Lane, Harrow, Middlesex, HA1, 3AF. United Kingdom Phone: 01-423-0688 Telex: 893667 **Hitachi Maxell, Ltd. Hong Kong Branch:** 506, World Commerce Centre, Harbour City, Phase 1, Canton Road, Kowloon, Hong Kong Phone: 3-689243 Telex: 55724 MXLHK **Hitachi Maxell, Ltd. Kuwait Office:** c/o M/S Supplying Store, W.L.L., PO. Box No. 1154, Kuwait, State of Kuwait Phone: 444882 Telex: MAX44122 KT **Hitachi Maxell, Ltd. Singapore Office:** c/o Hitachi (Singapore) Pte. Ltd., 18, Pasir Panjang Road, #01-03 PSA Multi-Storey Complex, Singapore 0511 Phone: 2730838 Telex: 21216

maximum at 5 V, is fully compatible with Intel Corp.'s iSBC 80/24 CPU board but uses much less power. The 80C85 microprocessor can be set to run at 2.42 or 4.84 MHz.

Sockets on the card allow the addition of up to 64-K bytes of Jedec-compatible EPROM. Two iSBX-compatible connectors are also on the card; a lithium battery ensures that data can be retained in RAM for five years.

A version of the CBC 85C/24 with 8-K bytes of static RAM will be available in this quarter in two temperature ranges—0° to 70°C and −40°C to +85°C. It will sell for $945.

Diversified Technology, 112 E. State St., P. O. Box 748, Ridgeland, Miss. 39158.
Phone (601) 856-4121 [Circle 355]

EMULATOR BUILDS BISYNCHRONOUS LINK

The PCNetwork/BSC 3270 GateWay, a bisynchronous connection system that links local-area networks to mainframes, has an open architecture based on the IBM Corp. Netbios session-layer interface. One IBM Personal Computer/XT or PC AT acts as the gateway, connecting the work stations on the net to the mainframe in the same manner as would an IBM 3270 cluster controller.

Each work station can operate as a 3270 display, 3270 printer or both concurrently. The system's special features include the HotKey, which allows users to switch between 3270 terminal emulation and DOS applications on the PC; a keyboard-mapping option that lets the user redefine keytips to standardize the variation in keyboards across PC and host computers; and a menu that allows users to configure the product. Up to 32 PC users on the BSC GateWay can concurrently access IBM host subsystems.

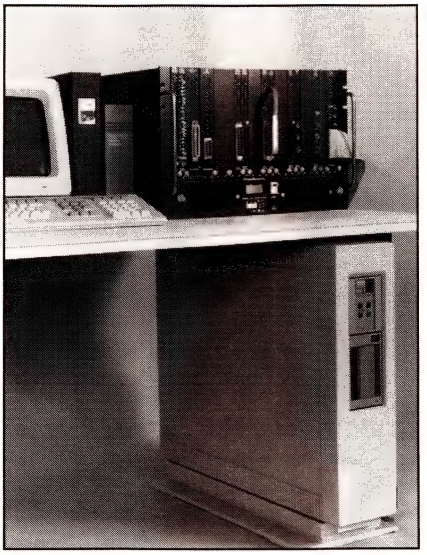
The PCNetwork/BSC 3270 GateWay sells for $2,495, and each work station costs $395. Quantity discounts are available. Delivery takes 30 days.

California Network Systems, 372 Turquoise St., Milpitas, Calif. 95035.
Phone (408) 943-9280 [Circle 372]

UNIT COLLECTS DATA FOR MICROVAX II

The 8040 Concept, a data-acquisition and process-automation system, connects Digital Equipment Corp.'s 32-bit MicroVax II work station with IEEE-583 Computer-Automated Measurement and Control hardware for access to the manufacturer's standard process-interface modules, crates, and accessories.

Operating under MicroVMS, the 8040 Concept handles processor-intensive, I/O-intensive, and real-time tasks. The



manufacturer also supports the 8040 Concept with PC/DBS, a process-control and data-base-system software package.

Available in both pedestal and rack-mounted configurations, the 8040 Concept includes the MicroVax II with 2 megabytes of memory, five serial lines, MicroVMS with eight user licenses, a 25-slot Camac crate and controller, and a Q-bus adapter. Prices for the system, without process-interface modules, start at $35,000, and delivery time is four to six weeks.

Kinetic Systems Corp., 11 Maryknoll Dr., Lockport, Ill. 60441.
Phone (815) 838-0005 [Circle 364]

PROCESSOR TRACKS 128 DATA STATIONS

In industrial settings, the intelligent TM900 transaction processor manages a network of up to 128 data-collection stations in an eight-line configuration. It also performs transaction prompting, validation and time stamping, and data buffering.

The TM900's factory multidrop network is optically isolated to improve common-mode noise rejection and eliminate ground-loop problems. A link port puts two of the transaction processors in communication with each other, with automatic switchover to provide a back-up in case one unit fails.

Options include a 10-megabyte hard disk and backup with an uninterruptible power supply. The 64-terminal version goes for $7,500 each, the 128-terminal version for $10,000. Quantity discounts are available and delivery time is two to four weeks.

Burr-Brown Corp., P. O. Box 11400, Tucson, Ariz. 85734.
Phone (602) 746-1111 [Circle 363]

DRAM CONTROLLER ACCESSES IN 150 NS

A 256-K-byte dynamic-RAM controller boasts a 150-ns maximum access time. Fabricated in CMOS, the VL4502 addresses and drives up to 2 megabytes of DRAM in 64- and 256-K-byte increments without external drivers.

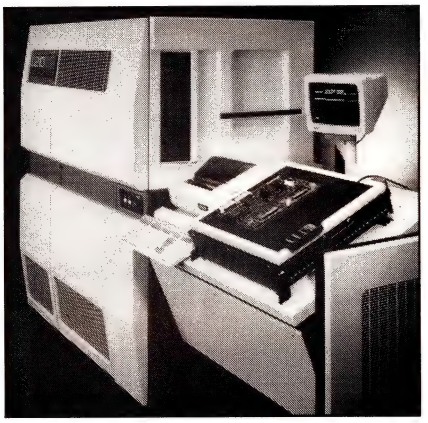
Low-power applications for the controller include portable computers and add-on memory boards for the IBM Corp. Personal Computer, as well as test and measurement units. It works in address multiplexing with an 18-bit multiplexer that provides the DRAM array with timing on up to nine lines.

The VL4502 is compatible with all major microprocessors, the company says, because it can run at 10 MHz with no wait states. It comes in 48-pin plastic and ceramic DIPs or in a 52-pin plastic leaded chip carrier and is TTL-compatible. In quantities of 1,000, the DRAM controller sells for $14.52. Volume orders will be filled immediately.

VLSI Technology Inc., 1109 McKay Dr., San Jose, Calif. 95131.
Phone (408) 942-1810 [Circle 367]

IN-CIRCUIT TESTER HAS 10-NS RESOLUTION

The L210i in-circuit test system for very large-scale-integration chips offers fast, clean signal edges for repeatable test results at pattern rates to 10 MHz. It supports up to 288 of these 10-MHz bidirectional test channels. The system has a 10-ns timing resolution for flexible, accurate specification of drive



phases and measurement windows.

The L210i uses three modules—a D8 channel card, an analog multiplexing subsystem, and MemTest, an option that enables embedded-memory testing at any one of the 3,024 test pins.

The user can easily upgrade the system in the field by swapping channel cards, and the company will give information on options. Pricing ranges from $350,000 to $450,000. A typical system includes 2 megabytes of memory, 1,000 test pins, software, and a 165-megabyte hard disk drive.

Teradyne Inc., 321 Harrison Ave., Boston, Mass. 02118.
Phone (617) 482-2700 [Circle 366]

CMOS GATE ARRAYS CARRY RAM ON CHIP

The UH family of 1.5-μm CMOS gate arrays contains three members: a 10,000-gate device with 12-K of on-chip RAM, a 15,000-gate device with 6-K of on-board RAM, and a 20,000-gate device with no RAM. Each version is fabricated in a triple-metal process that results in a smaller die size than double-metal technology produces. Housed in pin-grid-array packages with 256 pins, the parts fit into minimal pc-board space.

Typical gate delays are less than 1 ns. The family's dual-port RAM saves on addressing circuitry in many applications, and the access time for the array's RAM is typically 15 ns.

Fujitsu will accept UH-family designs in the first quarter of 1986, for production in the second quarter. Pricing varies according to the design.

Fujitsu Microelectronics Inc., Marketing Communications, 3320 Scott Blvd., Santa Clara, Calif. 95054.
Phone (408) 727-1700 [Circle 357]

GATE ARRAYS OFFER HIGH-CURRENT CELLS

For digital applications, the HCD series of gate arrays provides up to 1,500 equivalent gates with a maximum of 24 high-current—48 mA—I/O lines, and up to 56 standard—4.8 mA—I/O lines. The standard and high-current interface lines occupy the perimeter of the die and can be programmed as an input, an output, or a bidirectional buffer. Thus the series is well suited for both high- and low-drive interface applications. These include bus drivers, ribbon-cable drivers, and LED drivers. The arrays can be configured as voltage-controlled oscillators, digital-to-analog converters, comparators, and so on.

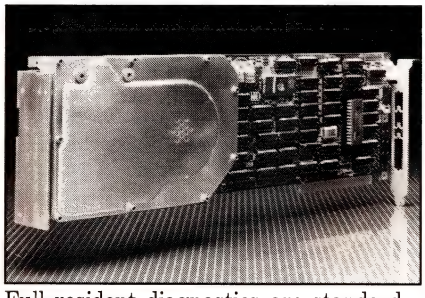
The gate arrays are implemented in 3-μm silicon-gate CMOS technology and come in both leaded chip carriers and small-outline packages for surface mounting, or in DIPs. Pricing and delivery information are not available.

Array Technology, 1297 Parkmoor Ave., San Jose, Calif. 95126.
Phone (408) 297-3333 [Circle 358]

HARD DRIVE FITS ON PLUG-IN CARD

The HC 2045, a turnkey product for the IBM Corp. Personal Computer, PC/XT, and compatibles, is a 3½-in. Winchester disk drive on a board with a 20-megabyte capacity and an average access time of 45 ms.

The HC 2045, which also contains an embedded controller, plugs directly into a standard slot and draws less than 9 W from the computer's power supply. The Winchester drive can withstand a 40-g shock if dropped when not operating.



Full resident diagnostics are standard.

The HC 2045 sells for under $1,000. Delivery is scheduled to start sometime next month.

AK Associates, P. O. Box 69, Manhattan Beach, Calif. 90266.
Phone (213) 379-9616 [Circle 370]

BUBBLE MEMORY HOLDS 512-K BYTES

The PBU 85E, an intelligent bubble-memory board, has a capacity of 256- or 512-K bytes of nonvolatile memory. It matches a standard half-height floppy drive in both size and mechanical fit.

The unit provides nonvolatile solid-state memory storage in the temperature range of 0° to +55°C (–20°C to +70°C is optional), suiting it for program loading or data storage. The PBU 85E holds data in formatted software-selectable blocks of 512 or 128 bytes, permitting use in a block-random-access mode. Access times averages 36 ms for a block of 512 bytes. The unit features an RS-232-C interface and is compatible with several bit-oriented protocols, including Higher Data Link Control, Synchronous Data Link Control, and Digital Equipment Corp.'s TU58 Tape RSP.

The board connects to the host computer through a number of standard serial ports with selectable 75- to 38.4-kb/s interface rates. The unit has a single 5-V power supply, built-in power-failure detection, and no cooling requirements, as well as built-in self-diagnostics and status indicators.

The PBU 85E standard unit costs $2,619. Delivery is from stock.

Plessey Microsystems Inc., 1 Blue Hill Plaza, Pearl River, N. Y. 10965.
Phone (914) 735-4661 [Circle 369]

FLASH ADC ACHIEVES 11-BIT RESOLUTION

Micro Power Systems used its bulk-silicon molybdenum-gate CMOS process to build a monolithic flash analog-to-digital converter with 11 bits of resolution. Replacing hybrid flash converters that cost considerably more, the MP7685 sells for only $319 in quantities of 100.

The MP7685 two-layer interconnection technology is based on a refractory metal molybdenum with low 0.2-Ω/square resistance, resulting in time delays of only 0.5 ps per 10-μm length. By connecting two converters in series, designers can achieve 12-bit resolution. To double the 2-MHz part's speed, two MP7685s can be connected in parallel.

The MP7685 dissipates just 150 mW operating from a 5-V supply. The part comes in die form, 40-pin DIPs, or in chip carriers. Delivery takes up to four weeks.

Micro Power Systems Inc., 3100 Alfred St., Santa Clara, Calif. 95054.
Phone (408) 727-5350 [Circle 359]

BIPOLAR ADCs RUN AT 30 MEGASAMPLES/S

Three bipolar analog-to-digital converters provide a conversion rate of 30 million samples/s and operate from a single 5-V power supply. The manufacturer recommends the flash converters for use in video-signal processing, digital instrumentation, robotics, and other applications in which high-speed data conversion is needed.

The HA19216 incorporates 6-bit latched data outputs and clock-input terminals that are TTL- and CMOS-compatible. The HA19210 and HA19209 8-bit ADCs, which are also TTL- and CMOS-compatible, feature a typical power dissipation of 250 mW.

Samples of all three are available now, with production quantities to follow this quarter. The 6-bit model will sell for $14.40 each in quantities of 1,000, the 8-bit parts for $36 in ceramic packages and $26.40 in plastic in the same quantity.

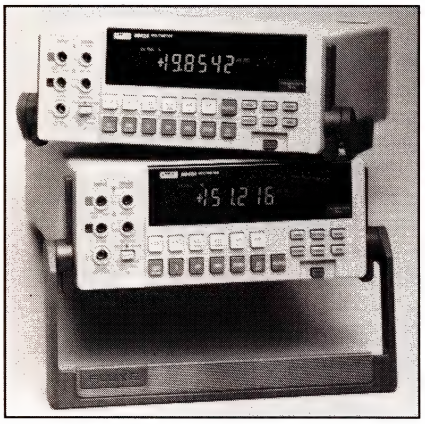
Hitachi America Ltd., Semiconductor & IC Division, 2210 O'Toole Ave., San Jose, Calif. 95131.
Phone (408) 942-1500 [Circle 360]

MULTIMETER IS ACCURATE TO 0.003%

The 8842A, a 5½-digit multimeter for such measurement applications as production test or research and development, has a basic accuracy within 0.003% for dc and 0.08% for ac. The meter also features 100-nV resolution for dc voltage measurements, 1-μA resolution for dc current measurements, and 100-μΩ resolution for resistance tests.

The multimeter is hermetically sealed and will stay calibrated for two years. Three rack-mounting kits are available for single- or dual-meter applications. The 8842A also has an adjustable tilt bail/handle for bench use. It sells for $995 and will be available in January.

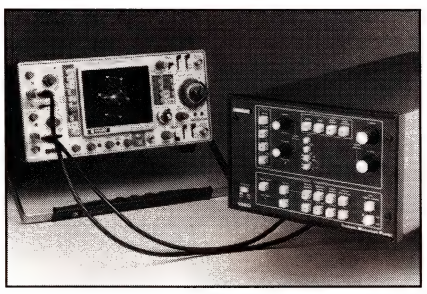
John Fluke Manufacturing Co., P. O. Box C9090, Everett, Wash. 98206.
Phone (800) 426-0361 [Circle 368]



VIDEO TEST PACKAGE COMBINES GEAR

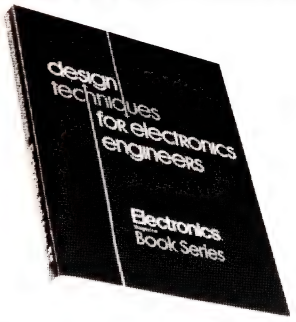
The 1520 integrated measurement package (IMP) for testing video systems combines a waveform monitor and vectorscope with a test-signal generator in a single package. It features an automatic "signal follows measurement" mode; 14.3-MHz, 10-bit, digitally synthesized test signals; source identification through 12-character overlay of signals; and an optional audio reference tone.

The 1525 IMP display monitor (pictured), the display device for the 1520 IMP, has a 6-in. CRT with 12-kV accelerating voltage that provides a bright, sharp trace. The monitor includes a pow-



7.
Low power consumtion
Extremely low power consumtion of only 75 mW without fixed polarity of current means a lower circuit power demand and less heat dissipation.
75mW
MT Relay
For a reliable future.
For further information and address of your local sales representative please contact:
Standard Telephon and Radio AG
Components Division
8027 Zurich/Switzerland
Tel. 01 201 42 55, Telex 815 385
ITT
Circle 75 on reader service card

DESIGN TECHNIQUES
for
ELECTRONICS ENGINEERS



Expert guidance at every point in the development of engineering project-making measurements, interpreting data, making calculations, choosing materials, controlling environment, laying out and purchasing components, and interconnecting them swiftly and accurately. Nearly 300 articles from *Electronics'* "Engineer's Notebook," with more than 500 diagrams and tables.

Order your copy today! Send $17.95 to:
P.O. Box 541
Hightstown,NJ 08520
609/426-5070

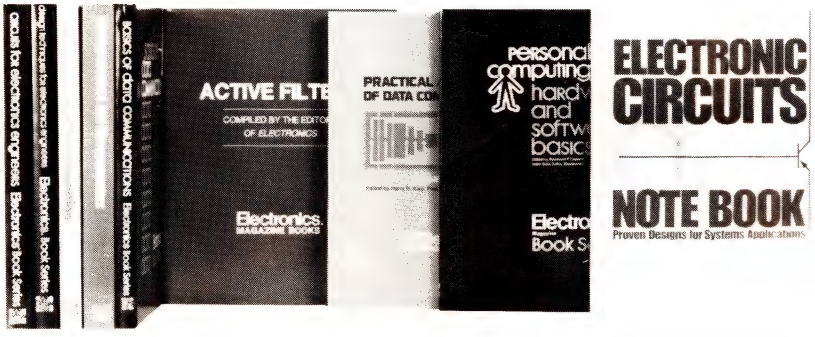
OR

McGraw-Hill
Int'l Publications Co.
Attn: ECC
McGraw-Hill House
Maidenhead, Berkshire SL6 2QL
England

Ten-day money-back guarantee. Allow 4 to 6 weeks for delivery.

Published by Electronics Magazine...

Books of special interest to our readers



Circuits for Electronics Engineers
Almost 350 diagrammed circuits arranged by 51 of the most useful functions for designers. Taken from the popular "Designer's Casebook" of *Electronics*, these circuits have been designed by engineers for the achievement of specific engineering objectives. Pub. 1977, 396 pages, softcover.
Order No. R-711, $17.95.

Electronic Circuits Notebook
Contains 268 completely illustrated electronic circuits conveniently arranged by 39 vital functions, including amplifiers, audio circuits, control circuits, detectors, converters, display circuits, power supplies and voltage regulators, function generators, memory circuits, microprocessors, and many others, as published in *Electronics* magazine 1977-1980. Companion volume to *Circuits for Electronics Engineers*. Pub. 1981, 344 pages, softcover.
Order No. R-026, $17.95.

Design Techniques for Electronics Engineers
Expert guidance at every point in the development of an engineering project—making measurements, interpreting data, making calculations, choosing materials, controlling environment, laying out and purchasing components, and interconnecting them swiftly and accurately. Nearly 300 articles from *Electronics*' "Engineer's Notebook," with more than 500 diagrams and tables. Pub. 1977, 370 pages, softcover.
Order No. R-726, $17.95.

Microelectronics Interconnection and Packaging
Articles from *Electronics* include sections on lithography and processing for integrated circuits, thick- and thin-film hybrids, printed-circuit-board technology, automatic wiring technology, IC packages and connectors, environmental factors affecting interconnections and packages, computer-aided design, and automatic testing. Pub. 1980, 321 pages, softcover.
Order No. R-927, $15.95.

Microprocessors and Microcomputers: One-chip Controllers to High-end Systems
Practical orientation to all aspects of microprocessors and microcomputers in 95 articles from *Electronics* covering low-end microcontrollers, mid-range microprocessors, high-performance 16-bit microprocessors, high-speed bipolar processors, peripheral support chips, signal processors, board-level microcomputers, software and applications. Pub. 1980, 482 pages, softcover.
Order No. R-011, $18.95.

Basics of Data Communications
This compilation of essential articles from *Data Communications* magazine includes chapters on terminals, acoustic couplers and modems, communications processors, networking, channel performance, data link controls, network diagnostics, interfaces, and regulations and policy. Pub. 1976, 303 pages, softcover.
Order No. R-608, $15.95.

Practical Applications of Data Communications
Selected articles from *Data Communications* magazine cover architecture and protocols, data-link performance, distributed data processing, software, data security, testing and diagnostics, communications processors, and digitized-voice and data-plus-voice. Pub. 1980, 424 pages, softcover.
Order No. R-005, $17.95.

Personal Computing: Hardware and Software Basics
More than 50 articles from leading publications provide information on personal computing hardware, software, theory and applications. Pub. 1979, 266 pages, softcover.
Order No. R-903, $15.95.

Active Filters
Covers the theory and practical implementation of filter networks built with active elements. Includes design tables and computer/calculator programs, as published in *Electronics*. Pub. 1980, 133 pages, softcover.
Order No. R-003, $11.95.

Order today using this coupon!

Electronics Magazine Books
P.O. Box 541
Hightstown, NJ 08520
609/426-5070

McGraw-Hill Intl. Publications Co.
European Circulation Center
Maidenhead, Berks. SL6 2QL, UK
(Tel 10628123431; Telex 848640)

Order #	Qty	Price
R-		$
R-		$
R-		$
R-		$
R-		$

Name

Title

Company

Street/PO address

City/State/Zip (Outside USA: City/postal code/country)

☐ Payment enclosed (Payment must accompany orders under $25. USA residents add applicable local tax.)
☐ Bill my company (or attach company Purchase Order)
☐ Bill me

Ten-day money-back guarantee applies on all books.

SOFTWARE

er cord, three 24-in. 75-Ω cables with BNC connectors, and three external graticules. The 1520 IMP and the 1525 IMP display monitor sell for $6,250. Delivery will begin in December.
Magni Systems Inc., 9500 S.W. Gemini Dr., Beaverton, Ore. 97005.
Phone (503) 626-8400 [Circle 377]

SOFTWARE WORKS ON MICROCOMPUTER CHIPS

Micro/OS, a real-time multitasking operating system for single-chip computers, provides documented time-, task-, and interrupt-management functions. The software frees the engineer from having to write program code from scratch; instead, he can concentrate on specific application software.

The software, which uses roughly 10% of the on-chip memory, permits as many as 16 tasks to share the CPU on a preemptive and prioritized basis. Typical functions include keypad scanning and display updating. Engineers using Micro/OS can design and develop program code in an organized, building-block fashion.

Prices for Micro/OS start at $250.
Micro Computer Control, P.O. Box 275, Hopwell, N.J. 08525.
Phone (609) 466-1751 [Circle 350]

BASIC VERSION HAS IEEE-488 SYNTAX

T-Basic, a technical engineering Basic for computer-aided-design applications, puts the emphasis on graphics and instrument control. It is the only language for personal computers that has built-in IEEE-488 interface syntax for working with both graphics and instrument peripherals, according to the manufacturer.

T-Basic permits software written for Hewlett-Packard Co. and Tektronix Inc. engineering computers to be adapted easily for personal computers. The software runs with popular operating systems, including PC-DOS, MS-DOS, C/PM, Unix, and VMS.

The language features complete error trapping as well as trace and debug facilities. Also featured is a full array of binary, scalar, array, matrix, and scientific mathematical functions, including standard trigonometric, transcendental, and other functions that use both integer and double-precision floating-point data.

Pricing for the T-Basic software package ranges from $495 to $1,995. Delivery is from stock.
TransEra Corp., 3707 N. Canyon Rd., Provo, Utah 84604.
Phone (800) 224-6550 [Circle 351]

SURFACE MOUNTING. A free, illustrated 32-page handbook on surface mounting gives an overview of the technology, then touches on issues in surface mounting confronting today's engineers. These include retention to the pc board, strain relief, thermal mismatch, lead design, insulator materials, and automated assembly and packaging. The booklet presents the technology's development in terms of designs, testing, and packaging of four of the company's "fast-track" headers and receptacles. Tables summarize surface-mount processes, their production capabilities, and thermal expansion coefficients. A glossary rounds out the handbook. To receive a copy, write to Molex Inc., 2222 Wellington Ct., Lisle, Ill. 60532, or call (312) 969-4550. [Circle reader service number 421]

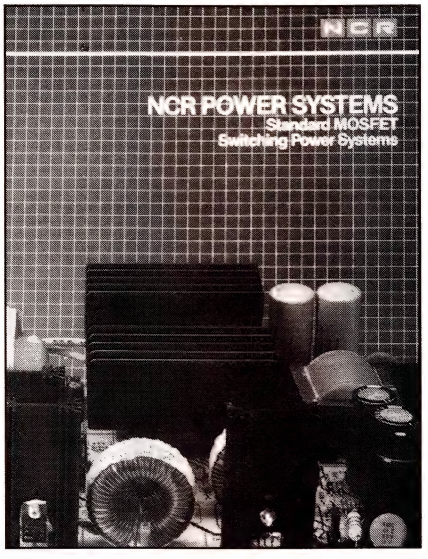
LOGIC DEVICES. A 248-page handbook is devoted entirely to erasable programmable logic for the designer. The text covers technology choices, software, development-system support, and performance considerations. Included are more than 140 pages of application information, with specific design examples. The company also includes data sheets for its entire product line. The *EPLD Handbook* is available for $7.95 from Altera Corp., 3525 Monroe St., Santa Clara, Calif. 95051; phone (408) 984-2800. [Circle 422]

VAX FACTS. Digital Equipment Corp. is sending out free literature on its recently introduced VaxStation II. An oversize color brochure sets forth the work station's principal features, stressing its compatibility with other VAX systems, the windowing capabilities of MicroVMS software, and its accessibility through DEC-net or IBM Corp.'s Systems Network Architecture protocols. Original-equipment manufacturers can fill out a card that comes with the brochure to receive more detailed information. The literature is available from DEC's OEM Group, 4 Mt. Royal Ave., UP02-3, Marlboro, Mass. 01752, or call (800) 344-4825. [Circle 423]

DYNAMIC RAM. A design-analysis report that describes the Intel i51256, a 256-K CMOS DRAM chip, presents complete circuit schematics as well as a description of each circuit's operation. The report from Mosaid Inc. also includes microphotographs, a chip floor plan, and other supporting information. Mosaid president Dick Foss says, "Anyone who thinks that CMOS automatically simplifies circuit design should study the i51256 very carefully." Call (408) 727-7199 for a free copy or write the company at 3375 Scott Blvd., Suite 130, Santa Clara, Calif. 95051. [Circle 424]

MACHINE AUTOMATION. A free 16-page, four-color guide to selecting plug-compatible machine controls and actuators discusses integration of motion, machine and process control, programming, and price-performance considerations. The products covered include three series of programmable controllers; a compatible operator's console; proximity sensors; compatible linear and rotary positioning tables; and more. Request this guide from Control Technology Corp., 25 South St., Hopkinton, Mass. 01748, or call (617) 435-9595. [Circle 425]

SWITCHERS. Standard MOS FET switching power systems for computers and peripherals—40 models in all—are described in a free catalog. The product line goes from 100 to 500 W, all with a demonstrated mean time between failures of 50,000 hours. All models meet international safety and electromagnetic-interference standards for data-processing equipment. Other standard features include protection against overload, overvoltage, and brownout; magnetic-switch technology; and power-fail signaling. The catalog gives operating specifications, power ratings, and voltage-current output levels for each model. Contact NCR Power Systems, 584 S. Lake Emma Rd., Lake Mary, Fla. 32746 to request a copy, or phone (800) 327-7612. [Circle 426]

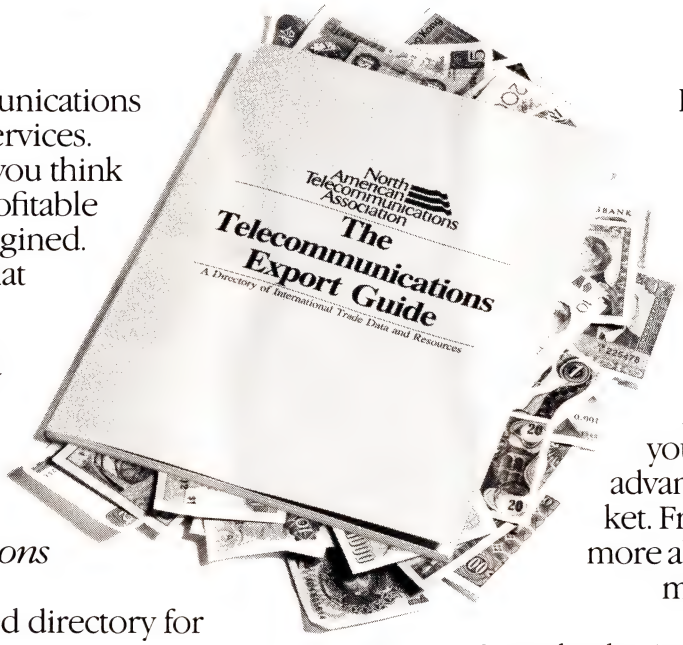


TUTORIALS. The IEEE Computer Society Press has issued its 1986 catalog of tutorials, conference proceedings, standards, and other items. Tutorials cover artificial intelligence, networks, industrial computers, parallel processing, database management, testing, and other current topics. They consist of reprints of articles by recognized experts in their fields. IEEE members will receive a discount on this publication. The society's address is 1730 Massachusetts Ave. N. W., Washington, D. C. 20036. Phone (800) 272-6657; in California, (714) 821-8380. [Circle 429]

MEASURING ERRORS. The model SE7205 high-density digital-recorder calibrator is described in a free six-page brochure. This is a self-contained unit designed for use with any high-density digital-recording tape recorder; it measures and displays data errors that occur while recording and reproducing digital data. The SE7205 also sets up recording parameters. The brochure gives specifications and summarizes the manufacturer's capabilities in high-density digital recording. Write to Thorn EMI Technology Inc., 8601 Dunwoody Pl., Atlanta, Ga. 30338, or phone (404) 587-0017. [Circle 428]

© 1985 NORTH AMERICAN TELECOMMUNICATIONS ASSOCIATIO

How to import money.


North American Telecommunications Association
The Telecommunications Export Guide
A Directory of International Trade Data and Resources

Export telecommunications equipment and services.

It's easier than you think and a lot more profitable than you ever imagined.

If you know what you're doing.

And everything you need to know is contained in one slim, easy-to-use volume –NATA's helpful *Telecommunications Export Guide.*

The just-updated directory for successful telecommunications exporters.

The *Export Guide's* got it all: opportunities, obstacles, strategies, indirect exporting, export and piggyback trading companies, establishing operations and distribution, creating an aggressive in-house export program.

Plus export profiles of 134 countries listed alphabetically, help available state-by-state (it varies a lot), a complete list of essential export publications, electrical plug types in use throughout the world and a whole lot more. In short, everything you need to know to take full advantage of this booming market. From the people who know more about telecommunications marketing than anyone else in the world–NATA.

Consider this: Telecommunications exports have leaped from less than $500 million in 1977 to well over a billion dollars last year. The price of buying-in is the modest price of the *Export Guide.* Need we say more?

North American Telecommunications Association

800-LET-NATA (800-538-6282)

Call 9-5 EDT Mon.-Fri.

Circle 78 on reader service card

Please send _____ copy(ies) of NATA's *Telecommunications Export Guide* immediately. I want to start taking advantage of this invaluable information resource right away.

☐ NATA member $85.00 per copy
☐ Non-member $115.00 per copy

For orders of 6 or more copies shipped to the same address, deduct $20.00 per copy. Add $2.00 per copy for postage and handling on all orders.

$_____ Total Payment

☐ Payment Enclosed ☐ Purchase order attached
☐ Charge my order to: ☐ MasterCard ☐ Visa

Account No._____

Interbank No. (MasterCard Only)_____

Expiration Date_____

Payment or purchase order required prior to shipment.

Name_____

Title_____

Company_____

Address_____

City_____ State_____ Zip_____

Signature_____

Mail your order to:
NORTH AMERICAN
TELECOMMUNICATIONS ASSOCIATION
P.O. Box 39989, Washington, DC 20016 (202) 296-9800

LETTERS

Prototype report premature

To the editor: There were several factual errors in a recent "Electronics Newsletter" item [*Electronics*, Oct. 21, 1985, p. 11], which reported on certain remarks I made as part of a presentation at the National Conference on Alternative Technologies for Class IV Computing in Golden, Colo.

In particular, the data relative to forthcoming engineering work stations, which I presented, referred to the general characteristics and the cost of work stations expected to become available in the 1986-87 time frame and not specifically to future IBM work stations. Contrary to what's reported in your newsletter, no such work station has been delivered as yet to UCLA, and no prototype has been installed.

The computer network now installed in the UCLA School of Engineering and Applied Science, with the aid of a substantial grant from IBM Corp., includes an IBM 4381, two IBM 4361s as well as a large number of IBM PC ATs. When advanced IBM work stations become available, these will be added to the network.

Walter J. Karplus
Professor, Computer Science Dept.
University of California, Los Angeles

In reply: *Professor Karplus's paper, which was not available at the conference, does indeed deal with the general characteristics of work stations. However, confusion apparently reigned at the conference when he fielded several questions from the audience about the IBM work station. Although his initial remarks were about general trends, the questions were specifically about IBM's coming system. It appeared that his responses were about IBM targets for the advanced work station.*

Moreover, when the presentation continued, Karplus indicated that an IBM work station had been installed on UCLA's computer network. He says that is not the case, but he left a contrary impression with his audience. The professor did say that the school plans to install about 60 advanced IBM work stations on its network once the machine is introduced next spring.

Correction

In the Oct. 28 profile on p. 57, we misspelled the name of Werner Englemayer, a researcher at AT&T Bell Laboratories' Interconnection Technology Group, Whippany, N. J., and a specialist in interconnection technology.

Advertisers Index

■	AMP Incorporated	10-11
	ATT Information	3C
	AT&T Information Systems	54-55
■	Boonton Electronics	2
	Data Translation	16
*	Fujitsu Ltd.	6E
	General Instrument	12
	Genrad	14
	Gespac Inc.	34
	Gnostic Concepts Inc.	66
	Grammar Engine	69
	Harris Semiconductor	61
*	Hitachi Maxell	8E
	Intel Corporation	21,23,25,27,29
	Interphase Corporation	46,47
	Intem Inc.	61
	Ironics	4
	ITT Intermetall	9
	ITT Standard	75
	Matrox Electronic Systems	4C
*	Melcher A.G.	4E
	Nata	78
	National Instruments	8
	National Semiconductor	2C,1
	NEC Corporation	6-7
	PEP	52-53
*	Rohde & Schwarz	1E
*	Siemens AG Munchen	2E,3E
	Texas Instruments, Incorporated	39-42
*	Toshiba	5E,7E

Classified and employment advertising

Brunelle Instruments, Inc.	70
ZTEC	70

■ For more information of complete product line see advertisement in the latest Electronics Buyers Guide
* Advertisers in Electronics International
‡ Advertisers in Electronics domestic edition

Advertising Sales Staff

Atlanta, Ga. 30319: Joseph Milroy
4170 Ashford-Dunwoody Road N.E.
[404] 252-0626
Boston, Mass. 02116:
M. E. "Casey" McKibben, Jr.
575 Boylston St.
[617] 262-1160
633-0155 Mobil Phone
Chicago, Ill. 60611: William J. Walker
[312] 751-3738
645 North Michigan Avenue
Cleveland, Ohio 44113:
[215] 496-3800
Costa Mesa, Calif. 92626: Fran Cowen
3001 Red Hill Ave. Bldg. #1 Suite 222
[714] 557-6292

Dallas, Texas 75240: Harry B. Doyle, Jr.
5151 Belt Line Road, Suite 907
[214] 458-2400
Englewood, Co. 80112: Harry B. Doyle, Jr.
7400 South Alton Court Suite 111
[303] 740-4633
Houston, Texas 77040: Harry B. Doyle, Jr.
7600 West Tidwell, Suite 500
[713] 462-0757
Los Angeles, Calif. 90010: Chuck Crowe
3333 Wilshire Blvd.
[213] 480-5210
New York, N.Y. 10020
Matthew T. Reseska [212] 512-3617
John Gallie [212] 512-4420
1221 Avenue of the Americas
Stamford, Ct. 06902
Albert J. Liedel
777 Long Ridge Road. Bldg. A
[203] 968-7115
Palo Alto, Calif. 94303:
Larry Goldstein, Jeffrey C. Hoopes,
Lauren Scott
1000 Elwell Court, [415] 968-0280
Philadelphia, Pa. 19102: Joseph Milroy
Three Parkway, [215] 496-3800
Pittsburgh, Pa. 15222: Matthew T. Reseska
Suite 215, 6 Gateway Center, [215] 496-3800
Southfield, Michigan 48075:
4000 Town Center, Suite 770, Tower 2
[313] 352-9760
San Francisco, Calif. 94111:
Larry Goldstein, Jeffrey C. Hoopes,
Lauren Scott
425 Battery Street
[415] 362-4600

Brussels: Art Scheffer
23 Chaussee de Wavre
Brussels 1040, Belgium
Tel: 513-73-95
Frankfurt/Main: Fritz Krusebecker, Dieter Rothenbach
19 Liebigstrasse, Germany
Tel: 72-01-81
Milan: Savio Pesavento
1 via Baracchini, Italy
Tel: 86-90-656
Paris: Jean - Christian Acis
17 Rue-Georges Bizet, 75116 Paris, France
Tel: (1) 47-20-33-42
Scandinavia: Andrew Karnig
Finnbodavagen
S-131 31 Nacka
Sweden
Tel. 46-8-440005
Telex: 17951 AKA S
Tokyo: Hirokazu Morita
McGraw-Hill Publications Overseas Corporation,
Kasumigaseki Building 2-5, 3-chome,
Kasumigaseki, Chiyoda-Ku, Tokyo, Japan
[581] 9811

United Kingdom: Art Scheffer
34 Dover Street, London W1
Tel: 01-493-1451

Business Department

Thomas E. Vachon
Director of Operations
[212] 512-2627
Leon Irgang
Circulation Director
[609] 426-5542
Frances M. Vallone
Reader Service Manager
[212] 512-6058

Thomas M. Egan
Production Director
[212] 512-3140
Carol Gallagher
Production Manager
[212] 512-2045
Evelyn Dillon
Production Manager Related Products
[212] 512-2044

Classified and Employment Advertising

[212] 512-2556

ELECTRONICS WEEK®

80386 TO GET A REAL-TIME OS

Though it is keeping mum on the exact number and names of developers, Intel Corp., Santa Clara, Calif., has announced that several companies have joined forces to develop a 32-bit real-time operating system to work with its new 80386 microprocessor and Multibus architecture. The only companies named publicly in the agreement are Mitsubishi Electric Corp. and Seiko Epson Corp., although Intel claims leading industrial-automation firms are also included. The product is not expected for at least a year.

SONY UNVEILS DISK CHANGER

Sony Corp. has beaten Eastman Kodak Co. to the punch in the rush to offer an optical high-speed data-retrieval system. Sony introduced its Writable Disk Auto-Changer system, which holds up to 50 12-in. optical disks for a total storage capacity of 164 gigabytes, last week at Comdex in Las Vegas. Kodak announced in May that it had such a system in the works. Sony's autochanger comes with proprietary robotics that retrieve the disks and insert them into one of two disk drives.

BOSCH, PHILIPS SWAP PRODUCTS

In a move to cut down overcapacity in Europe's consumer electronics industries, West Germany's Blaupunkt Werke GmbH, a member of the Robert Bosch Group of companies, and Grundig AG, under control of NV Philips of the Netherlands, are going to swap TV receivers and car radios. In addition, Blaupunkt has taken an option to acquire a 20% stake in Grundig. Under the agreement, Blaupunkt will phase out its production of TV sets and buy them from Grundig; Grundig, meanwhile, will stop making car radios, buying them from Blaupunkt.

A CHALLENGE IN LASER PRINTERS

Tokyo Electric Co., a Toshiba Corp. subsidiary, plans to give market leader Canon Inc. a challenge in the low-price laser-printer business. A representative says it is negotiating with Apple Computer Inc. and other manufacturers that want to sell customized versions of its LB-1301 prototype printer. Tokyo Electric claims that its private-label and original-equipment-manufacturer sales in the U. S. put it among the top three with Seiko Epson Corp. and Oki Electric Industry Co.

EIA ACCEPTED INTO CCITT

The Electronic Industries Association has been accepted as a participating organization in the International Telegraph and Telephone Consultative Committee, the group better known by its French acronym, CCITT. The CCITT's primary function is to write international administrative and technical standards for telecommunications services and equipment. The EIA's membership will open foreign telecom markets to U. S. companies, according to EIA president John J. McDonnell. The EIA represents about 100 U. S. telecom-equipment manufacturers.

RCA INFRARED CCD CAMERA IS READY

After more than a decade of development, RCA Advanced Technology Laboratories has announced it can produce a custom high-performance infrared charge-coupled-device camera. The camera's 160-by-244-element imaging array observes an entire scene at a time without mechanical scanning as in conventional units. It consists of more than 39,000 Schottky barrier charge-coupled diodes that take up a less than 0.5 in.^{2} and produce a standard TV-compatible image.

TAIWAN FIRM BIDS FOR 49% OF ESPRIT

Shareholders of Esprit Systems Inc., a Melville, N. Y., supplier of video-display terminals, will be asked to approve the sale of 49% of the company to its principal supplier, Advanced Datum Information Corp., Taipei, Taiwan. The deal involves 3.7 million shares of stock for $2.5 million and a $1.5 million product-purchase credit line. Esprit said the new funding, plus its bank credit line, would provide the working capital needed to finance its operations in the intermediate term.

EMPLOYEE COSTS TO STAY DOWN

Low inflation and a lackluster economy will combine to keep average salary increases low in 1986, according to a survey by the Hay Group, a Philadelphia management consultant. Hay warns that average increases could barely exceed the cost-price index—putting them in the 4% to 5% range. Cost control will also apply to other areas, says Hay. Some 24% of the companies polled used layoffs in the past year to cut costs. Another 20% froze hiring, and 19% used early retirement to reduce payrolls. In benefits, 23% increased their health-care deductibles during the year and another 20% raised employee contributions to their health-insurance premiums.

ALLIED-SIGNAL TO SPIN OFF 30 UNITS

Allied-Signal Inc., Morristown, N. J., is spinning off 30 business units into a new company to expedite their divestiture. Chairman Edward Hennessy Jr. said the spinoff will focus the giant conglomerate on three areas of specialization—aerospace and electronics, automotive, and advanced materials and chemicals. The new company has yet to be named, but will be led by Allied-Signal Inc. president Michael Dingman, who was chief executive at The Signal Companies Inc. before it was merged with Allied Corp. last spring. It will have assets worth about $3.2 billion at its inception. Hennessy also announced that Allied-Signal is instituting a plan to save an estimated $250 million by eliminating 3,000 jobs, most of them before Christmas.

HEX-FET MAKER SLASHES PRICES

With orders for power MOS FETs turning as soft as for other semiconductor components, market leader International Rectifier Corp. has chopped its prices up to 65% for larger devices, effective this week. The El Segundo, Calif., company holds about half the power MOS FET business with its Hexfet line and claims to be the most cost-efficient producer. Demand for MOS FETs turned weaker during the third quarter, observers note, and competitors are now selling hard. Motorola Semiconductor Products, the No. 2 MOS FET company, cut its prices sharply during the summer.

ERICSSON BUYS OUT VENTURE PARTNER

By year end, LM Ericsson of Stockholm will have full ownership of Ericsson Inc., its U. S. venture partner formed in 1980 with Atlantic Richfield Co. The Swedish telecommunications giant is paying $42 million for Arco's half of the operation, which is based in Richardson, Texas. Arco says the sale is part of a corporate restructuring program. Last year, Ericsson Inc. had sales of $500 million in telecommunications as well as wire and cable markets.

Now, AT&T brings more to CAD than just mice, monitors and modeling.

Any Computer Aided Design system lets you move lines on a monitor. But with the peace of mind an AT&T system can now bring you, those lines will seem to dance.

Because AT&T brings undisputed communications strengths and a new standard to CAD: We are delivering products designed to work in complete yet flexible systems. Moreover, these products will have the AT&T service and support to make them sound, long-term *investments*.

In CAD, this means you get equipment that works well. Equipment that works well together in a network. And equipment with the backing to keep working well far into the future.

AT&T introduces a growing family of advanced design workstations, developed in conjunction with Omnicad—an innovator in CAD/CAM software:

AT&T OMNIDRAFT.™ This is a workstation system for engineers, architects and draftsmen who need automated drawing capabilities. It uses proven CAD software, runs on the superior MS*DOS-based AT&T PC 6300 and comes bundled with complete AT&T service and support.

The Electronics CAD Family. Led by AT&T OMNIBOARDS,™ this is the first truly integrated ECAD system. Its modules include logic capture; packaging and placement; autorouting (available separately in AT&T OMNIROUTE™); and Computer Aided Manufacturing output capability. What's more, this high performance printed circuit board design system lets you connect workstations through standard industry networks.

The point is flexibility. And it's a big part of the thinking behind "The Computers With The Future Built In." It means the CAD system you choose today will work with whatever you may need tomorrow.

And it will all be supported by the same, single source.

If that sounds interesting, call us at 1 800 824-8824 (in New York State, 1 800 523-1019). Let us arrange a demonstration or put you in touch with an authorized AT&T Representative.

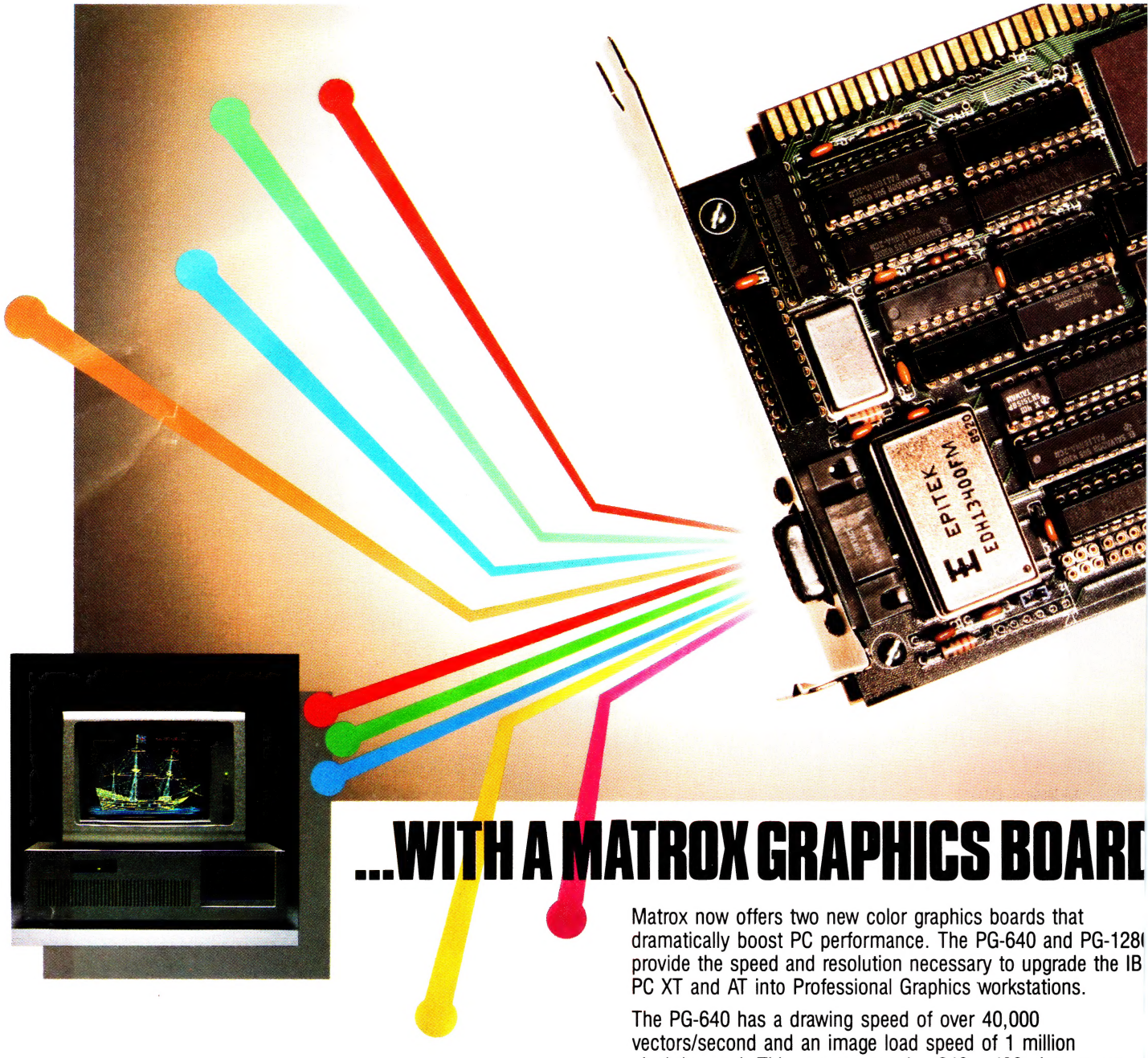
Now there's a CAD system that lets you draw on a lot more than just a monitor.

AT&T
The right choice.

*MS-DOS is a trademark of Microsoft Corp./© 1985 AT&T Information Systems

Circle 901 on reader service card

TURBOCHARGE YOUR PC's GRAPHICS



...WITH A MATROX GRAPHICS BOARD

- 640 x 480 x 8 display (PG-640)
- 1280 x 1024 x 8 display (PG-1280)
- 40,000 vectors/sec. drawing speed
- 100% IBM PGC compatible
- Full IBM CGA emulation
- 1 million pixels/second image load

Matrox now offers two new color graphics boards that dramatically boost PC performance. The PG-640 and PG-128(provide the speed and resolution necessary to upgrade the IB PC XT and AT into Professional Graphics workstations.

The PG-640 has a drawing speed of over 40,000 vectors/second and an image load speed of 1 million pixels/second. This means complex 640 x 480 pictures are drawn in under a second. The PG-1280 provides even faster picture updates, and displays four times the detail, 1280 x 10(pixels.

Both the PG-640 and PG-1280 are 100% compatible with IBM Professional Graphics card, and offer full Color Graphics Adapter emulation. All existing software runs without change

If you are interested in a 10 times performance boost:

CALL TOLL FREE 1-800-361-4903

Circle 902 on reader service card

matrox

1055 St. Regis Blvd.
Dorval, Quebec, Canada
H9P 2T4
Tel: (514) 685-2630
Tlx: 05-822798

IBM, IBM PC XT, IBM PC AT, PGC, CGA are trade marks of International Business Machines